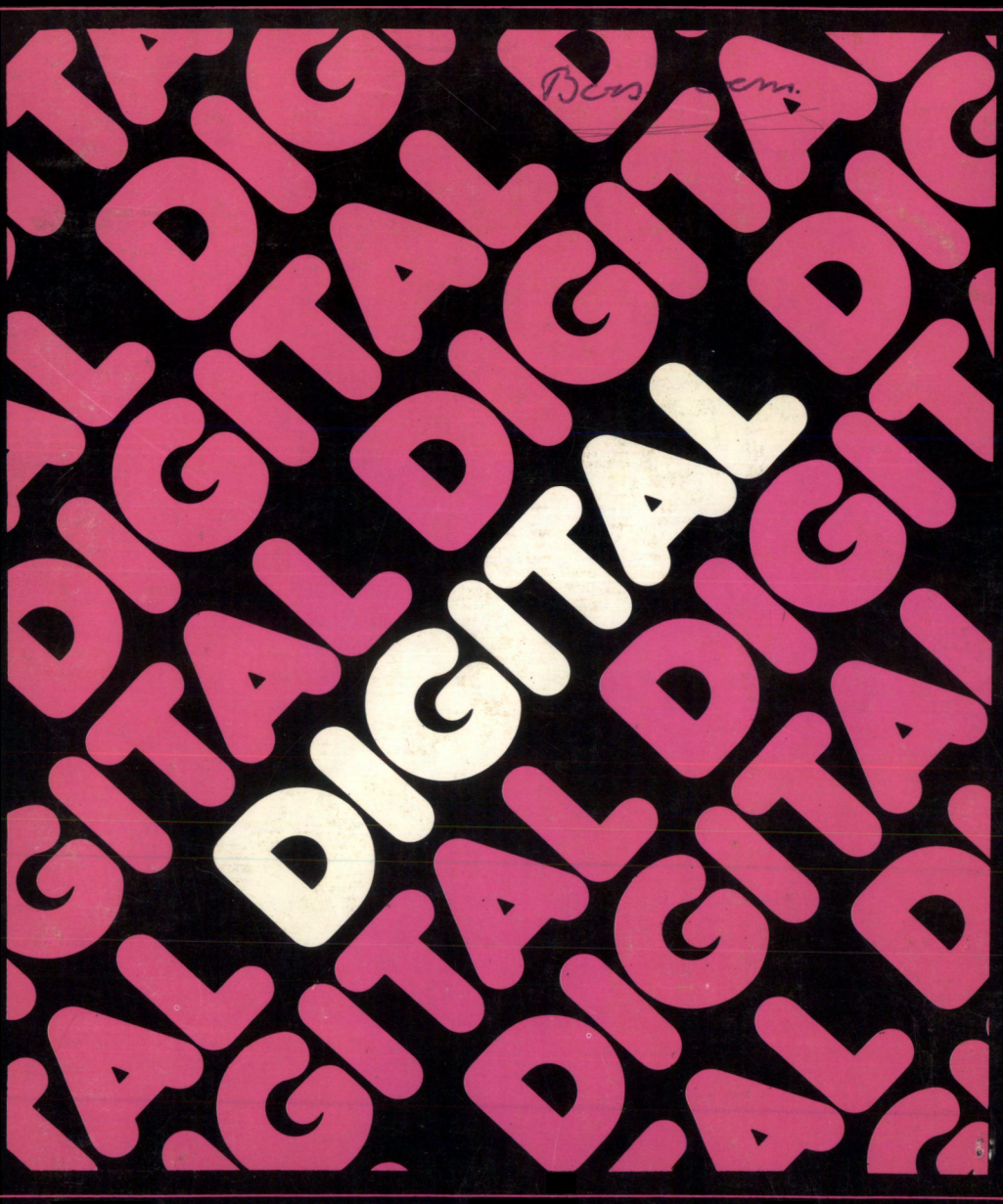

Integrated Circuit Databook

PLESSEY
SEMICONDUCTORS

ERRATA

The following devices are available *only* in DILMON package (code DC) : SP8613/4/5/6, SP8617/9, SP8634/5/6/7, SP8665/6/7, SP8675/6/7 and SP8735/6. All other SP8000 series devices in dual-in-line packages are available in ceramic DIL (code DG).

digital integrated circuits

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DEVICE TYPE

technical data

PLESSEY
SEMICONDUCTORS

SP520 SERIES
PROCESS CONTROL CIRCUITS

SP520B
GRAY CODE COUNTER

The SP520 digital integrated circuit is an RTL 5-bit up/down counter in positive logic with both Gray code and natural binary code TTL-compatible outputs. Other inputs and outputs use modified RTL to give improved noise immunity.

SP520 counters can be cascaded by suitable external connections to give a counter with any multiple of 5 bits. The counter is of a non-overflow design and will operate with an input frequency in excess of 1MHz. It can be reset to the 00000 state and the Gray O/Ps can be inhibited for "wired OR" applications.

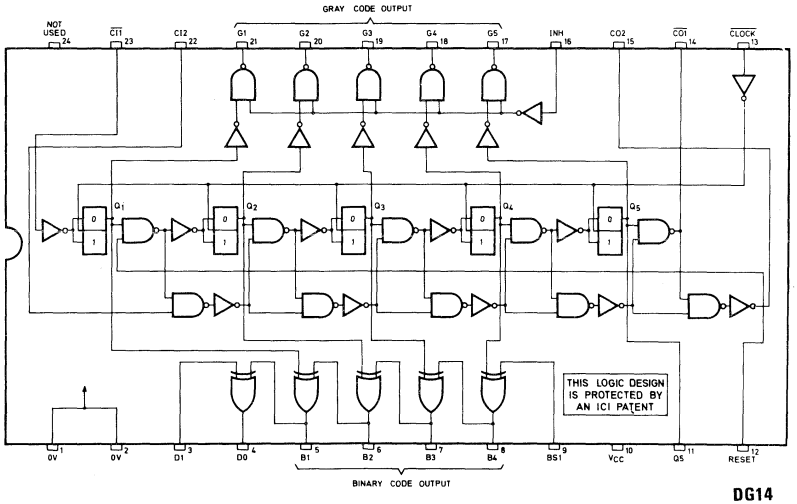


Fig.1 Logic diagrams

Pin No.	Function	Pin No.	Function
1	Common rail (0V)	14	Inhibit carry O/P to 1st flip-flop of next counter (C_{O1})
2	Common rail (0V)	15	Enable carry O/P to gate chain of next counter (C_{O2})
3	Counter external direction control (Logic '0' = up)	16	Inhibit I/P for all Gray O/Ps except auxiliary Gray code O/P Bit 5 (INH)
4	Binary code O/P direction (D_O)	17	Gray code O/P Bit 5 (G5)
5	Binary code O/P Bit 1 (B1)	18	Gray code O/P Bit 4 (G4)
6	Binary code O/P Bit 2 (B2)	19	Gray code O/P Bit 3 (G3)
7	Binary code O/P Bit 3 (B3)	20	Gray code O/P Bit 2 (G2)
8	Binary code O/P Bit 4 (B4)	21	Gray code O/P Bit 1 (G1)
9	Binary code I/P Bit 5 (B5I)	22	Enable gate chain I/P (CI_2)
10	Positive supply rail (V_{CC})	23	Inhibit I/P to 1st flip-flop (CI_1)
11	Auxiliary Gray code O/P Bit 5 (Q5)	24	No connection
12	Reset I/P for all flip-flop stages (forces 00000 state)		
13	$\overline{\text{Clock}}$ I/P		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C

V_{CC} = 5.0V ±0.25V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
INPUT REQUIREMENTS					
Counter external direction control (pin 3), Binary code I/P bit 5 (pin 9), and Enable gate chain I/P (pin 22):					
Input voltage 'High'	3.0			V	
Input voltage 'Low'			1.0	V	
Input current			25	μA	V_{in} = 3.0V
Inhibit I/P for Gray O/Ps (pin 16)					
Input voltage 'High'	3.0			V	
Input voltage 'Low'			1.0	V	
Input current 'High'			250	μA	V_{in} = 3.0V
Input current 'Low'			50	μA	V_{in} = 1.0V
Reset I/P for all flip-flops (pin 12)					
Input voltage 'High'	2.3			V	with voltage drive
Input voltage 'Low'			0.8	V	with voltage drive
Input current			3.5	mA	with voltage drive
Input current 'High'	1.0			mA	With current drive
Clock I/P (pin 13)					
Input voltage 'High'	3.0			V	See note 1
Input voltage 'Low'			1.0	V	
Input current			200	μA	V_{in} = 3.0V
Input clock frequency			1	MHz	1:1 mark = space ratio
Input slew rate	20			V/μs	See note 2
Inhibit I/P to 1st flip-flop (pin 23)					
Input voltage 'High'	2.3			V	See note 3
Input voltage 'Low'			0.8	V	
Input current			2.0	mA	T_{amb} = +70°C, V_{in} = 2.3V
Input slew rate	20			V/μs	See note 2
OUTPUT CHARACTERISTICS					
Binary code O/P bits 1-4 (pins 5-8)					
Output voltage 'Low'			0.4	V	Sink current = 6.4mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state		6.0	8.0	kΩ	
Binary code O/P direction (pin 4)					
Output voltage 'Low'			0.4	V	Sink current = 6.4mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			2.6	kΩ	
Aux. Gray code O/P bit 5 (pin 11)					
Output voltage 'Low'			0.4	V	Sink current = 3.2V
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			8.0	kΩ	
Gray code O/Ps bits 1-5 (pins 17-21)					
Output voltage 'Low'			0.4	V	Sink current = 8.0mA
Output voltage 'High'		4.2		V	I_{out} = 0mA
Output impedance in 'High' state			3.4	kΩ	
Output leakage to earth in inhibited state			20	μA	T_{chip} = 100°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Inhibit carry O/P to 1st flip-flop of next counter					
Output voltage 'Low' **(pin 14)**			0.4	V	R_{pd} = 4kΩ (see notes 4 and 5)
Output voltage 'High'	2.4	2.75	3.2	V	
Enable carry O/P to gate chain of next counter					
Output voltage 'Low' **(pin 15)**			0.4	V	Sink current = 3.2mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			4.8	kΩ	
Power supply drain current (pin 10)		70	96	mA	V_{CC} = 5.0V, clock I/P = 0V

NOTES

1. In the high state the input level affects the overall power consumption. The chip power consumption increases by approximately 12.5mW and it might therefore be desirable to limit the clock input voltage with, say, a zener diode.
2. The flip-flops need fast edges for reliable toggling.
3. In the high state the input current is directly proportional to the input voltage and increases at approximately 1mA/V. It might therefore be desirable to limit the maximum input voltage.
4. An emitter follower output will not sink current and is not therefore suitable for interfacing directly with TTL or DTL.
5. This output is an emitter follower with no internal pulldown resistor — when counters are cascaded the emitter follower pulldown is provided by the next stage.

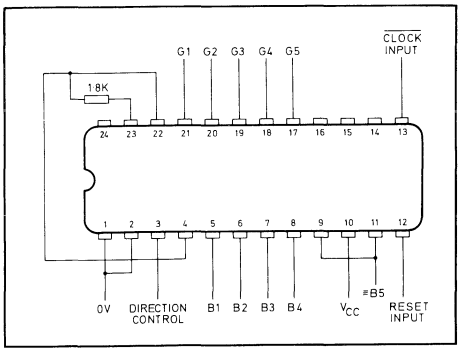


Fig.2 SP520 connected as a 5-bit counter

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage	+7V
Continuous +ve input voltage	not greater than the supply voltage in use
Max. operating junction temp	+175°C
Storage Temperature	−50°C to +175°C

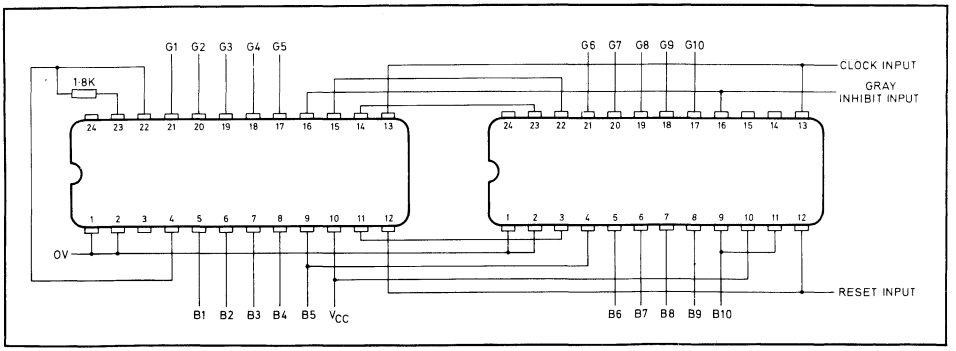
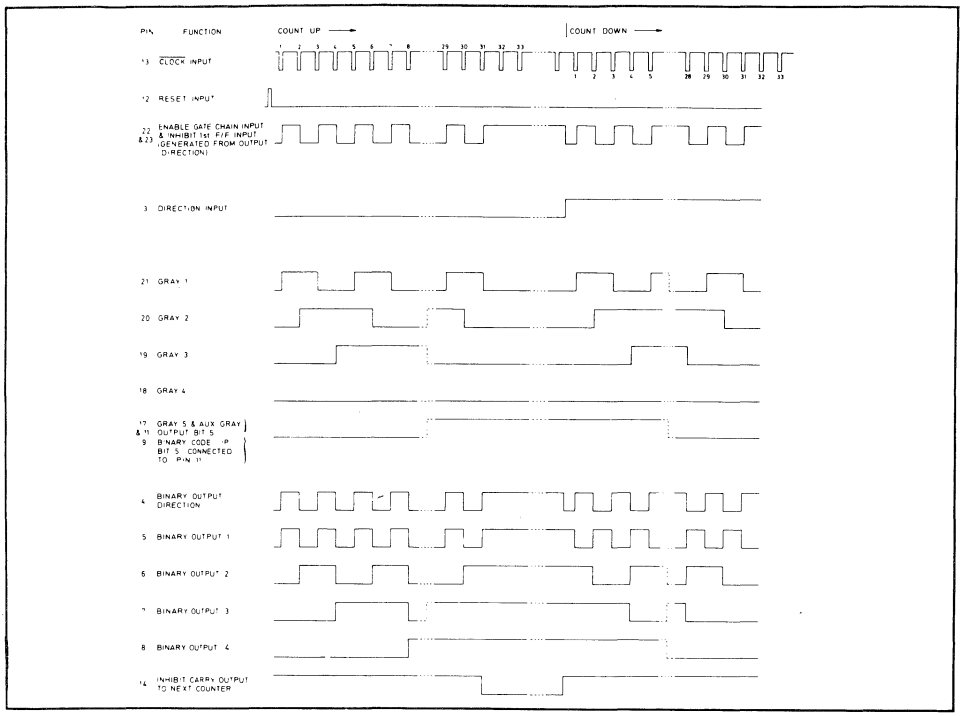


Fig.3 Two SP520s connected as a 10-bit counter



The enable gate chain output is normally in the '0' state and goes to the '1' state only when all the Gray outputs are low and the enable input high.

Fig.4 Logic states for 5-bit counter

PLESSEY
SEMICONDUCTORS

SP520 SERIES
PROCESS CONTROL CIRCUITS

SP521B
BINARY RATE MULTIPLIER

A binary rate multiplier (BRM) is a form of programmable divider in which the number of pulses appearing at the output for each full period of the counter is equal to the value of the binary number present on the binary inputs. Thus, if the binary word input to a BRM is, say, 10101 (=21) then, for every 32 clock pulses counted only 21 will be gated onto the output.

The SP521 is a binary rate multiplier with two sets of binary control inputs, each associated with its own clock phase. The phase 1 controls operate in conjunction with the counter chain clock (ϕ1). The phase 2 controls operate in conjunction with a separate clock (ϕ2) which can be antiphase with ϕ1 clock and interlaced with it. Phase 1 and phase 2 outputs can be combined by wiring them together.

The operating temperature range of the SP521 is 0°C to +70°C and the nominal supply voltages are 0V and +5V. The device ,is available in 24-lead D.I.L 0.6 inch spacing ceramic packages.

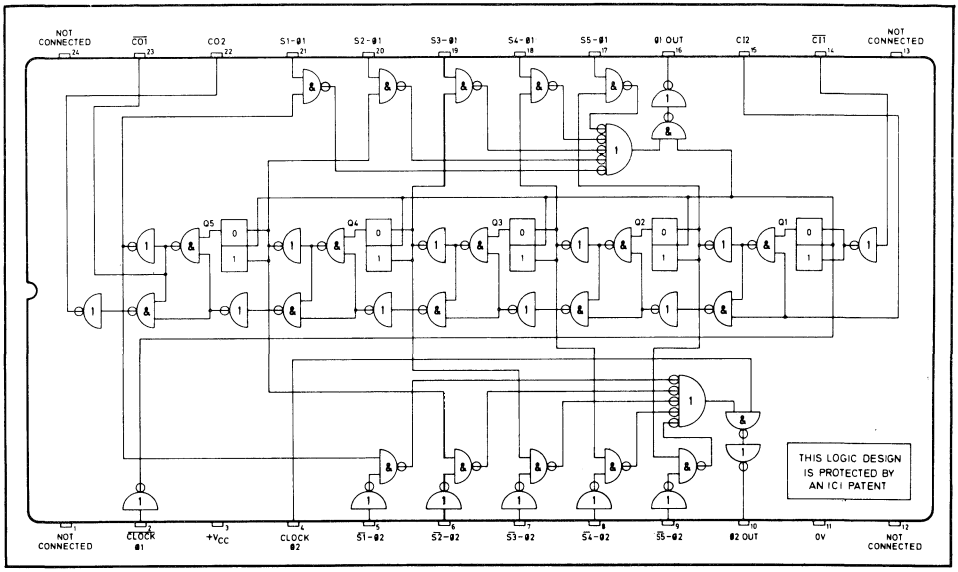


Fig.1 Logic Diagram

DG14

OPERATING NOTES

The phase 1 controls operate in conjunction with the master clock pulses of the BRM counter chain (ϕ1 clock). The inputs operate with true positive logic and have CCSL-compatible input requirements. The phase 2 controls have standard RTL type inputs and operate with inverse positive logic in conjunction with the ϕ2 clock.

Phase 1 and phase 2 outputs are emitter followers with non-standard logic levels – the logic levels being set by the logic levels of the phase 1 inputs and the ϕ2 clock input respectively. In a multiple-package BRM (i.e. > 5 bits) the phase 1 outputs are wired together to give the required output. If the ϕ2 clock input is interlaced with the ϕ1 clock, the phase 2 outputs can be wire-ORed with the phase 1 outputs to give a continuous pulse train. The maximum ϕ1 and ϕ2 clock input frequency is in excess of 1MHz

PIN CONNECTIONS

Pin No.	Function	Pin No.	Function
1	No connection	14	Inhibit I/P to 1st flip-flop (CI_1)
2	Clock I/P $\phi 1$ (BRM drive)	15	Enable gate chain I/P (CI_2)
3	Positive supply rail (V_{CC})	16	Phase 1 O/P ($\phi 1_{OUT}$)
4	Clock I/P $\phi 2$	17	Phase 1 Binary Control Input (true) Bit 5 ($S5\phi 1$)
5	Phase 2 Binary control input (inverse) Bit 1 ($\overline{S1}\phi 2$)	18	Phase 1 Binary Control Input (true) Bit 4 ($S4\phi 1$)
6	Phase 2 Binary control input (inverse) Bit 2 ($\overline{S2}\phi 2$)	19	Phase 1 Binary Control Input (true) Bit 3 ($S3\phi 1$)
7	Phase 2 Binary control input (inverse) Bit 3 ($\overline{S3}\phi 2$)	20	Phase 1 Binary Control Input (true) Bit 2 ($S2\phi 1$)
8	Phase 2 Binary control input (inverse) Bit 4 ($\overline{S4}\phi 2$)	21	Phase 1 Binary Control Input (true) Bit 1 ($S1\phi 1$)
9	Phase 2 Binary control input (inverse) Bit 5 ($\overline{S5}\phi 2$)	22	Enable carry O/P to gate chain of next BRM (CO_2)
10	Phase 2 O/P ($\phi 2_{OUT}$)	23	Inhibit carry O/P to 1st flip-flop of next BRM (CO_1)
11	Common Rail, 0 volts	24	No connection
12	No connection		
13	No connection		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Tamb = 0°C to +70°C
V_{CC} = 5.0V ±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
INPUT CONDITIONS					
Clock $\overline{\phi 1}$ I/P pin 2					
Input voltage 'high'	3.0			V	See note 1
Input voltage 'low'			1.0	V	
Input current			200	µA	V_{IN} = 3.0V
Input slew rate	20			V/µS	See note 2
Clock $\phi 2$ I/P (pin 4)					
Input voltage 'high'	3.1			V	
Input voltage 'low'			1.0	V	
Input current			150	µA	V_{IN} = 3.1V
Binary phase 1 control inputs, bits 1 to 5 (pins 17 to 21)					
Input voltage 'high'	3.1			V	See note 3
Input voltage 'low'			1.0	V	
Input current			20	µA	V_{IN} = 3.1V
Phase 2 Binary control inputs, bits 1 to 5 (pins 5 to 9)					
Input voltage 'high'	1.0			V	Voltage drive
Input voltage 'low'			0.5	V	
Input current			0.5	mA	V_{IN} = 1V
Input base resistor	1.0			kΩ	
Input current 'high'	200			µA	Current drive
Inhibit I/P to 1st flip-flop (pin 14)					
Input voltage 'high'	2.0			V	See note 1
Input voltage 'low'			1.0	V	
Input current			2.0	mA	V_{IN} = 2.0V
Input slew rate	20			V/µS	See note 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Enable gate chain I/P (pin 15)					
Input voltage 'high'	3.1			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 3.1V
OUTPUT CHARACTERISTICS					
Phase 1 and phase 2 O/P's (pins 10 & 16) (Emitter follower outputs. See notes 3 and 4.)					
Output high level	3.0			V	Phase 1 I/Ps & Clock 02 I/P connected to V_{CC}(+5V) via 8 kΩ resistor. R_{pd} = 4kΩ
Output low level			0.4	V	
Enable carry O/P to gate chain of next BRM (pin 22)					
Output low level			0.4	V	Sink current = 1.6mA
Output high level		V_{CC}		V	I_{OUT} = 0mA
Output impedance			4.4	kΩ	
Inhibit carry O/P to 1st flip-flop of next BRM (pin 23)					
Output voltage 'high'	2.1		3.1	V	R_{pd} = 4kΩ
Output voltage 'low'			0.8	V	See note 4
Power supply drain current (pin 3)		35	60	mA	V_{CC} = +5V, Clock 01 I/P = 0V Inhibit I/P = 0V

1. In the high state these inputs affect the overall chip power consumption. In the case of the clock $\phi 1$ input the power consumption increases with increasing input voltage level at approximately 12.5 mW/V. In the case of the Inhibit I/P to 1st flip flop the input current is directly proportional to the input voltage in the high state, and increases at approximately 1mA/V.
2. The flip-flops need fast input edges for reliable toggling.
3. The voltage levels of the high states of the phase 1 and phase 2 outputs depend on the input voltages of the phase 1 binary inputs and the clock $\phi 2$ input respectively. In each case the output voltage level will be approximately $2V_{BE}$ more positive than the appropriate input voltage. These outputs have no internal pulldown resistors.
4. An emitter follower output will not sink current and is not therefore suitable for interfacing directly with TTL or DTL.

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage (V_{CC})	+7V	Operating ambient temperature	0°C to +70°C
Continuous +ve input voltage	not greater than the supply voltage in use	Storage temperature	−50°C to +175°C

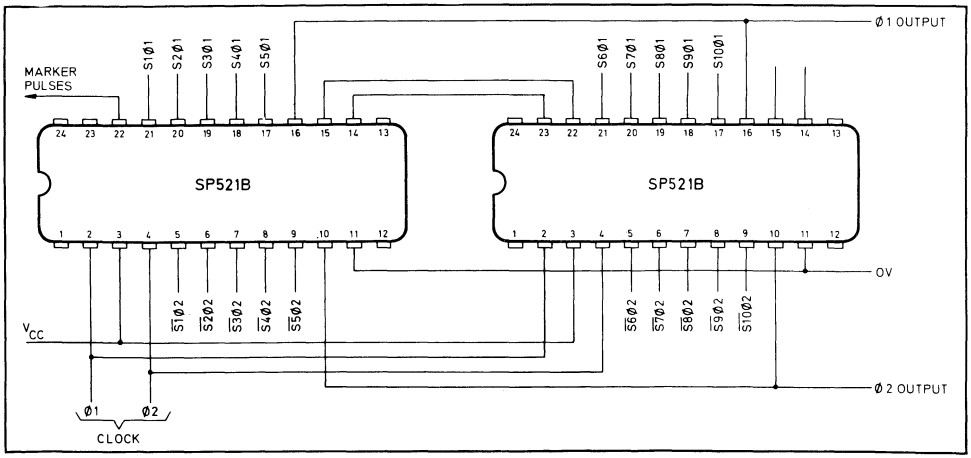


Fig.2 Two SP521s connected as a 10-bit BRM (packages viewed from above)

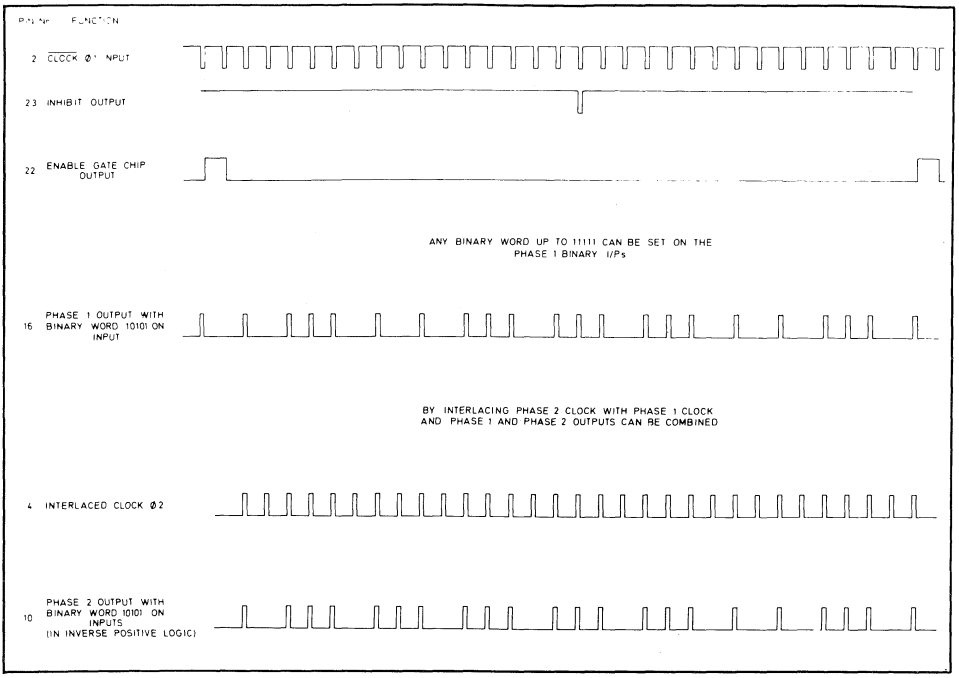


Fig.3 SP521 logic states (5-bit BRM). Enable gate chain input held at logic '1', Inhibit 1st flip-flop held at logic '0'.

PLESSEY
SEMICONDUCTORS

SP520 SERIES
PROCESS CONTROL CIRCUITS

SP522B
PHASE LOCK, DIVIDER & COMPARATOR

The SP522B is the most specialised of the SP520 series of RTL digital integrated circuits. It contains a frequency divide-by-eight and interlacing circuit, a frequency comparator and digital filter, and an input phase-locking circuit.

Frequency divider

The clock input frequency of the dividing circuit is referred to as 8f. An output is provided at a quarter of the clock frequency (2f), and 2 interlaced outputs are provided at one eighth of the clock frequency, 1fϕ1 and 1fϕ2. The maximum clock frequency of the divider chain is in excess of 2MHz.

Frequency comparator and filter

The frequency comparator is a five-state up/down counter which can be reset to the central symmetrical state. The reset input to the comparator is NORed with the 1fϕ1 signal. There is one count up input to the counter and two alternative count down inputs, one of which is compatible with CCSL logic. Two direction outputs are provided and one difference frequency output.

When the counter has been set into the central state by the reset there must be a difference of three pulses between the count up and count down inputs before there is a pulse in the difference frequency output. This means that a small amount of jitter in one input relative to the other will not appear at the output.

Phase lock circuit

The phase lock circuit accepts a random phase input (e.g. from a flowmeter transducer) and locks it to the phase of the master clock (8f input). The maximum frequency at which the phase lock circuit will work satisfactorily is 3.2f. A race condition can occur on switching on, but if the master clock and the input signal are phase independent it clears itself very quickly. The phase-locked output at pin 3 is intended to be used as the count up input to the frequency comparator, and is then connected externally to pin 10.

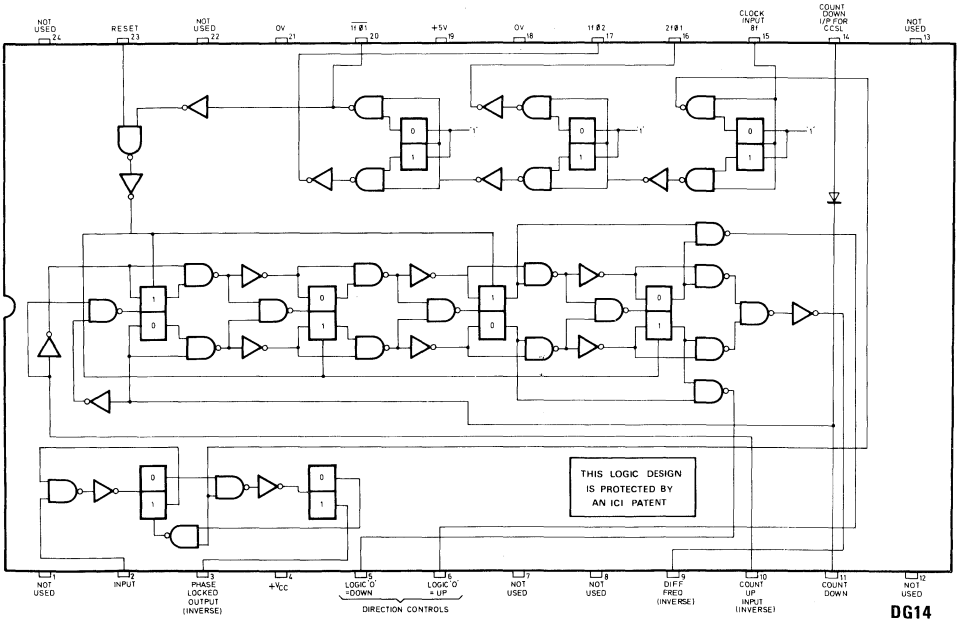


Fig. 1 SP522B Logic diagram

PIN CONNECTIONS

Pin No.	Function	Pin No.	Function
1	No connection	13	No connection
2	Input frequency signal (inverse phase)	14	Additional comparator count down I/P for CCSL logic
3	Phase lock O/P (inverse phase)		
4	Positive supply rail $+V_{CC}$	15	Master clock I/P (8f)
5	Direction control O/P (logic '0' = down)	16	2f ϕ1 O/P
6	Direction control O/P (logic '0' = up)	17	1f ϕ2 O/P
7	No connection	18	Common rail 0V
8	No connection	19	Positive supply rail $+V_{CC}$
9	Difference frequency — comparator O/P (inverse phase)	20	1f ϕ1 O/P
		21	Common rail 0V
10	Comparator count up I/P (inverse phase)	22	No connection
11	Comparator count down I/P	23	Reset comparator I/P (true)
12	No connection	24	No connection

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 0°C$ to $+70°C$
$V_{CC} = 5.0V \pm 0.25V$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
INPUT CONDITIONS					
Input frequency signal (pin 2)					See note 1
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	$V_{IN} = 2.7V$
Input slew rate	1			V/μS	See note 2
Comparator count-up input (pin 10)					
Input voltage 'high'	0.95			V	Voltage drive
Input voltage 'low'			0.5	V	Voltage drive
Input current		0.75	1.0	mA	$V_{IN} = 0{,}95V$
Input base resistor	420			Ω	
I/P current 'high'	150			μA	Current drive
Comparator count-down I/P (pin 11)					
Input voltage 'high'	1.0			V	Voltage drive
Input voltage 'low'			0.5	V	Voltage drive
Input current		1.0	2.0	mA	$V_{IN} = 1.0V$, $T_{amb} = 70°C$
Input base resistor	350			Ω	
Input current 'high'	900			μA	Current drive

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Additional count down I/P (pin 14)					
Input voltage 'high'	2.2			V	
Input voltage 'low'			1.0	V	
Input current			30	μA	V_{IN} = 2.2V
Master clock I/P (pin 15)					
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 2.7V
Input slew rate	1			V/μS	See note 2
Reset comparator I/P (pin 23)					
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 2.7V
OUTPUT CHARACTERISTICS					
Phase Lock O/P (pin 3)					See note 4
Output 'low'			0.4	V	Sink current = 1.6mA
Output 'high'	1.1			V	I_{OUT} = 0mA
Output impedance in high state			7.2	kΩ	
Direction control O/PS (Pins 5 & 6)					
Output 'low'			0.4	V	Sink current = 1.6mA
Output 'high'		V_{CC}		V	I_{OUT} = 0mA
Output impedance in high state			6.5	kΩ	
Difference frequency-comparator O/P (pin 9)					
Output voltage 'high'	3.1	3.5	3.8	V	
Output voltage 'low'		0.0	0.4	V	See note 5
2f ϕ1 O/P (pin 16)					
Output voltage 'low'			0.4	V	Sink current = 1.6mA
Output voltage 'high'		V_{CC}		V	I_{OUT} = 0mA
Output impedance in high state			5.2	kΩ	
1f ϕ2 O/P (pin 17)					
Output voltage 'high'	3.5			V	
Output voltage 'low'			1.0	V	See note 5
1f ϕ1 O/P (pin 20)					
Output voltage 'high'	3.1		3.8	V	
Output voltage 'low'		0.0	0.4	V	See note 5
Power supply drain current		70	82	mA	V_{CC} = 5V

NOTES

1 There is a 25% probability of a race condition occurring in the phase lock circuit when power is first applied. To ensure that the circuit is brought into its correct operating condition an input clock transition ('1' → '0') must occur while the 4fϕ1 clock is in the logic '1' state. In most systems, where the input clock and the master clock are not synchronous, this happens very quickly.

2 The input flip-flops need fast edges for reliable toggling.

3 For the count-down input there is an option of an RTL input (pin 11) or a CCSL compatible input (pin 14). When the RTL input is used the CCSL input should be connected to the 0V rail. When the CCSL input is used, the RTL input should be left open circuit.

4 The logic '1' level of this output is very low and is only suitable for driving an RTL input directly. If required, however, special interface techniques (such as grounded base, emitter input cascode type circuit) can be used to extract the O/P from this pin without further loading the logic '1' level.

5 Pins 9, 17 and 20 are emitter follower outputs and will not sink current. These outputs are not therefore suitable for interfacing directly with TTL or DTL.

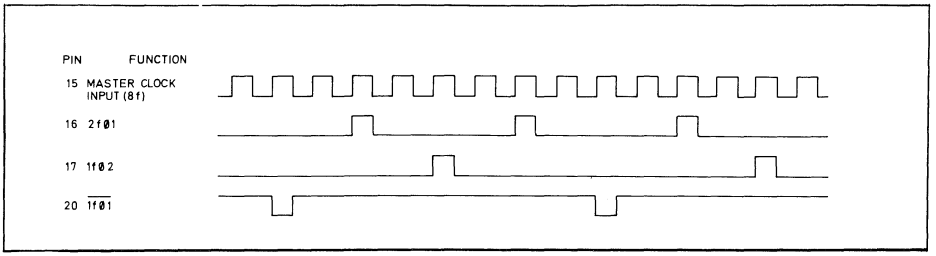


Fig. 2 Frequency divider logic timing

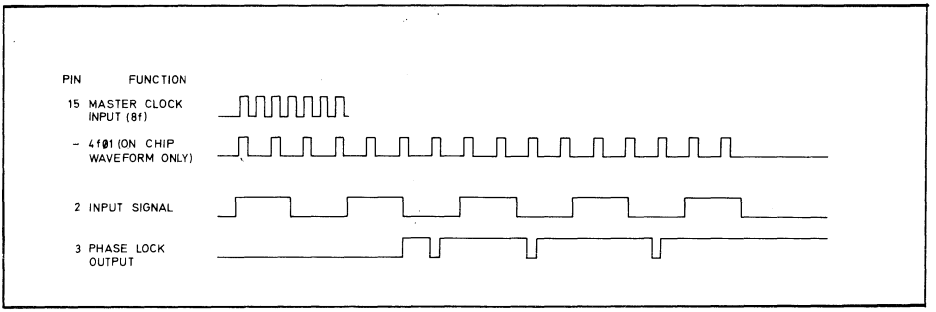


Fig. 3 Phase lock timing, illustrating recovery from race condition

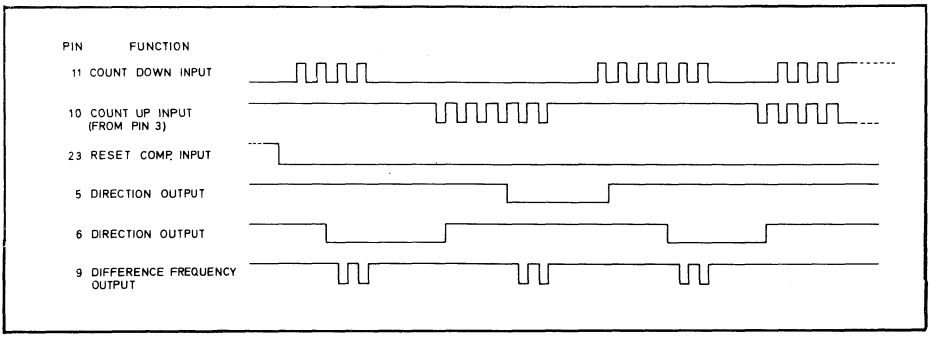


Fig. 4 Frequency comparator and filter timing

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage	+7V
Continuous +ve input voltage	not greater than the supply voltage in use
Operating ambient temperature	0°C to +70°C
Storage temperature	−50°C to +175°C

APPLICATION NOTES

Fig. 5 shows a 10-bit frequency-to-digital encoder using the SP522B together with other elements of the SP520 series. The encoder provides continuous parallel digital output in non-ambiguous Gray code, and is capable of giving an immediate correct response to an interrogation signal at any time. This application note should be read in conjunction with the SP520B and SP521B data sheets.

The encoder employs the continuous feedback principle. The input frequency is first phased-locked to the master clock input to the SP522B then applied, together with the feedback frequency from the binary rate multiplier (SP521B), to the frequency comparator in the SP522B. Any difference frequency that results is applied to the clock inputs of the SP520B Gray code counter. A direction control signal is also applied to one SP520B (least significant 5 bits) to determine the up/down mode of the counter.

Binary-coded outputs from the SP520B's form the numerical multipliers that determine the number of output pulses in each cycle (i.e. the feedback frequency) of the binary rate multipliers.

The feedback frequency is taken from pin 16 of each SP521B to pin 14 of the SP522B and is in phase with the 1fϕ1 clock signal. The phase 2 outputs of the SP521B's (pin 10) are in phase with 1fϕ2 clock and are interlaced with the main feedback frequency signal when pins 10 and pins 16 are wired-ORed. Negative binary inputs (pins 5 to 9 on each SP521B) determine the number of pulses in this stream and can therefore be used to provide a zero elevation facility.

The Gray code outputs of each SP520B are interrogated by taking the 'inhibit Gray output' (pin 14) to logic '0'; the outputs can, however, be continuously displayed using the binary-coded outputs (pins 5 to 9) to drive numerical indicators via a suitable interface.

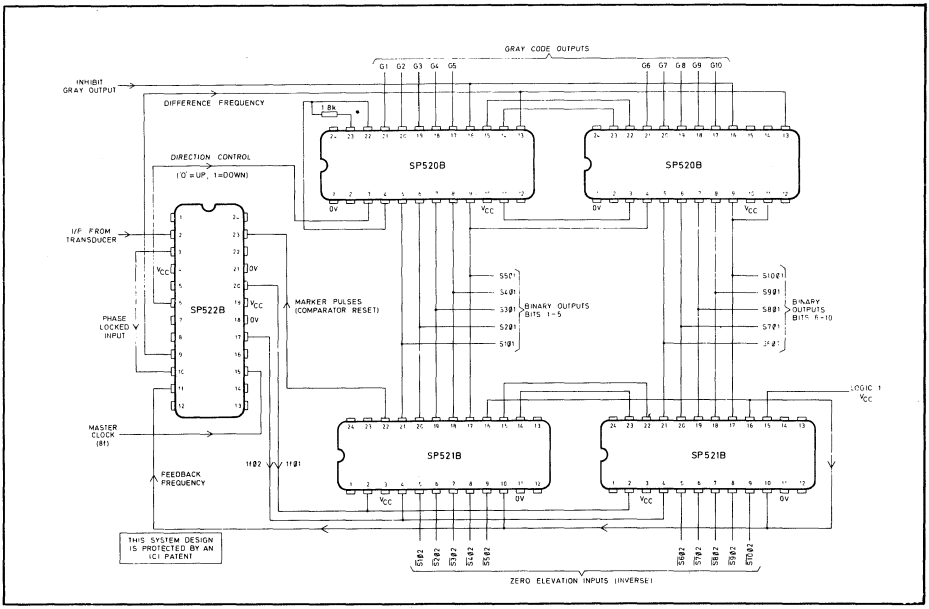


Fig. 5 Frequency-to-digital encoder

PLESSEY
SEMICONDUCTORS

SP530 SERIES
INDUSTRIAL LOGIC

SP530A
DUAL 3-INPUT AND/NAND GATE

The SP530A is a member of a family of high noise immunity industrial logic elements designed for easy use, without the need for external protection, by fabricating the circuits on the Plessey High Voltage Process, which has voltage breakdowns in excess of 90V. This process also has a special diffusion for the construction of buried avalanche diodes, which are capable of absorbing powerful noise transients without being destroyed.

Each circuit incorporates its own internal, regulated power supply, enabling it to work with large variations of voltage and high levels of noise and ripple on the external supply.

Each input is protected from the destructive power of RF noise by a high power avalanche diode connected between the input and ground. Each input also sources a current in excess of 1mA, so that a mechanical switch can be used as a logic input.

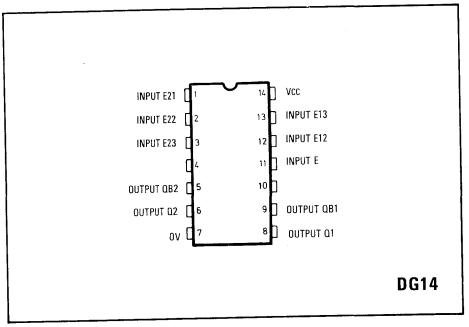


Fig. 1 Pin connections (top)

FEATURES

- Very High Noise Immunity
- Input Protection Against Destructive High Energy Noise Transients
- Ability to Work from Unregulated Poorly Smoothed Power Supply
- Ability to Drive 35mA Load Connected to External Supply
- Fan In and Fan Out of 10
- Logic Inputs Which Supply Currents for Reliable Use With Mechanical Switches

APPLICATIONS

- Process Control Logic
- Automatic Machine Control
- Logic Circuitry in Telephone Exchanges
- Any Situation where High Noise Levels or High Voltage Requirements Cause Problems for Standard Logic Ranges

QUICK REFERENCE DATA

	Min.	Max.	Units
+Vcc Power Supply Voltage			
Continuous	32	60	V
Transient		90	V
Power Supply Current		19	mA
Open Circuit Input Voltage	22	26	V
Short Circuit Input Current	1	3	mA
Output Saturation Voltage (35mA)		1.6	V
Input Threshold	12	17	V

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb}: —20°C to + 70°C
V_{CC}: 32V to 60V
Pins 13 and 1 connect to 0V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Power supply drain current			19	mA	V_{in} = 0V for all inputs
Open circuit input volts	22		26	V	V_{CC} = 38V to 60V
Short circuit input current	1		3	mA	V_{CC} = 38V to 60V
Input breakdown voltage	26		55	V	
Input logic levels					
Logic 1	—0.4		12	V	
Logic 0	17		26	V	
Output logic levels					
Logic 1			1.6	V	I_{out} = 35mA
Logic 0 (leakage)			10	μA	V_{out} = 20V
Dynamic Characteristics					
Output rise and fall times 20%–80%			300	μs	Output load: fan-out of 10 + 500pf
Delay to rise 50%-50%			300	μs	Input levels: logic 1 = 12V, logic 0 = 17V
Delay to fall 50%-50%			300	μs	Transition times <10μs

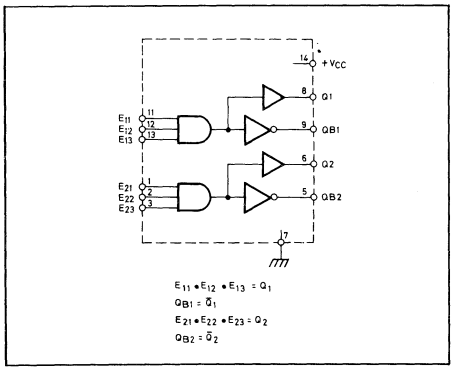


Fig. 2 Functional diagram (negative logic is assumed)

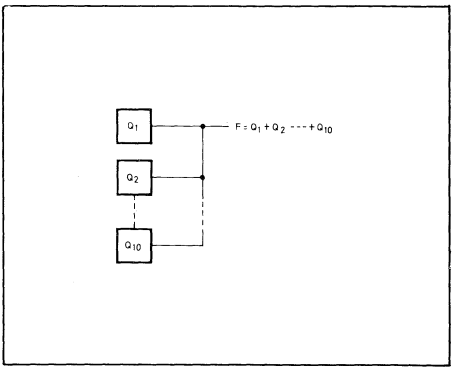


Fig.3 Wired -OR function

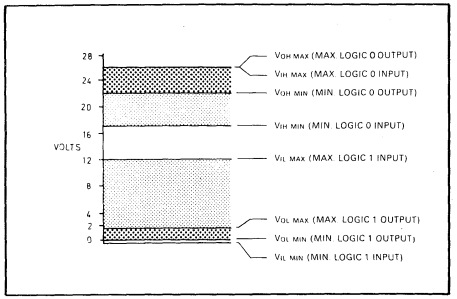


Fig. 4 Logic levels

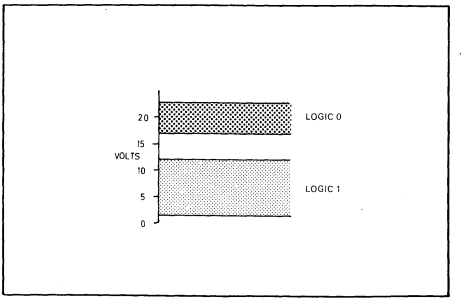


Fig. 5 Worst case DC noise margin: fanout/fan in of 10

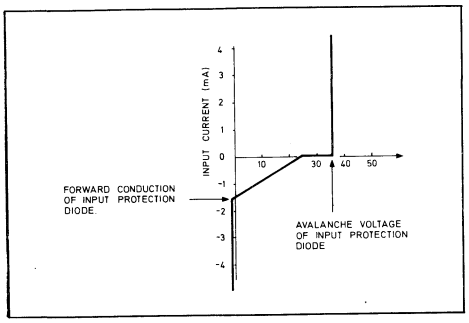


Fig. 6 Typical input characteristic

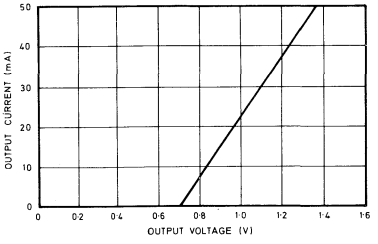


Fig. 7 Typical output characteristic

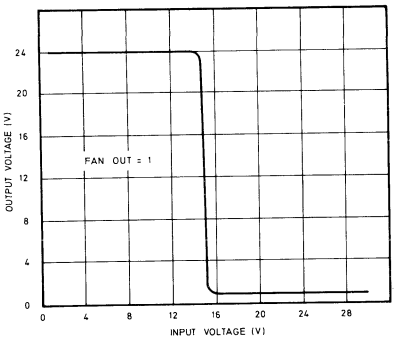


Fig. 8 Typical transfer characteristic for an inverting output: fanout=1

OPERATING NOTES

Up to ten outputs from any of the SP530 logic family may be connected together to form an OR function. One output or up to a 10 wide wired OR output may be used to drive up to 10 inputs.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Operating ambient temperature	−20°C to +70°C
Peak supply surge rating peak for 10ms	90V

PLESSEY
SEMICONDUCTORS

SP530 SERIES
INDUSTRIAL LOGIC

SP531A
DUAL 2-INPUT OR GATE

The SP531A is a member of a family of high noise immunity industrial logic elements designed for easy use, without the need for external protection, by fabricating the circuitsbon the Plessey High Voltage Process, which has voltage breakdowns in excess of 90V. This process also has a special diffusion for the construction of buried avalanche diodes, which are capable of absorbing powerful noise transients without being destroyed.

Each circuit incorporates its own internal, regulated power supply, enabling it to work with large variations of voltage and high levels of noise and ripple on the external supply.

Each input is protected from the destructive power of RF noise by a high power avalanche diode connected between the input and ground. Each input also sources a current in excess of 1mA, so that a mechanical switch can be used as a logic input.

The SP531 is a dual 2-input OR gate, with unusual non-standard outputs. The output devices form a undirectional switch controlled by the logic inputs. With the negative end of the outputs connected to 0V they are capable of driving a 35mA load connected to the external power supply, or may be used as perfectly standard logic outputs. However, they may also be stacked in series to form a wired-AND function with the bottom-most output connected to 0V.

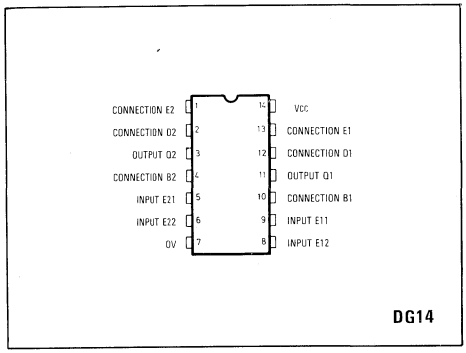


Fig. 1 Pin connections

APPLICATIONS

- Process Control Logic
- Automatic Machine Control
- Logic Circuitry in Telephone Exchanges
- Any Situation where High Noise Levels or High Voltage Requirements Cause Problems for Standard Logic Ranges

FEATURES

- Very High Noise Immunity
- Input Protection Against Destructive High Energy Noise Transients
- Ability to Work from Unregulated Poorly Smoothed Power Supply
- Output Wired-AND Facility
- Ability to Drive 35mA Load Connected to External Supply
- Fan In and Fan Out of 10
- Logic Inputs Which Supply Currents for Reliable Use With Mechanical Switches

QUICK REFERENCE DATA

	Min.	Max.	Units
+Vcc Power Supply Voltage			
Continuous	32	60	V
Transient		90	V
Power Supply Current		15	mA
Open Circuit Input Voltage	22	26	V
Short Circuit Input Current	1	3	mA
Output Saturation Voltage (35mA)		1.6	V
Input Threshold	12	17	V

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb}: —20 C to + 70C
V_{CC}: 36V to 60V
Pins 13 and 1 connect to 0V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Power supply drain current			15	mA	V_{in} = 0V for all inputs
Open circuit input volts	22		26	V	V_{CC} = 38V to 60V
Short circuit input current	1		3	mA	V_{CC} = 38V to 60V
Input breakdown voltage	26		55	V	
Output breakdown voltage	60			V	@ 10μA
Input logic levels					
Logic 1	—0.4		12	V	
Logic 0	17		26	V	
Output logic levels					
Logic 1			1.6	V	I_{out} = 35mA
Logic 0 (leakage)			10	μA	V_{out} = 20V
Dynamic Characteristics					
Output rise and fall times 20%–80%			300	μs	Output load: fan-out of 10 + 500pf
Delay to rise 50%-50%			300	μs	Input levels: logic 1 = 12V, logic 0 = 17V
Delay to fall 50%-50%			300	μs	Transition times <10μs

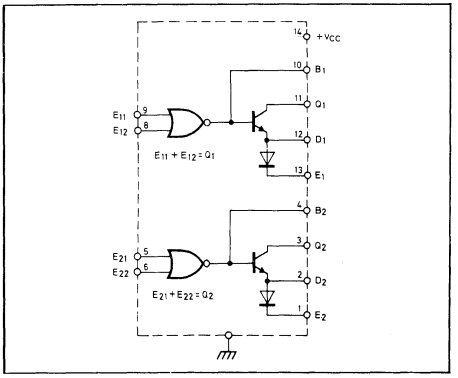


Fig. 2 Functional diagrams (negative logic is assumed)

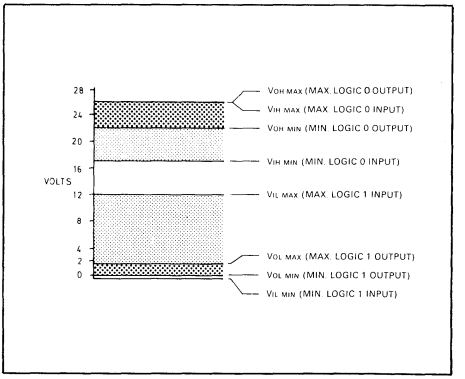


Fig. 3 Logic levels

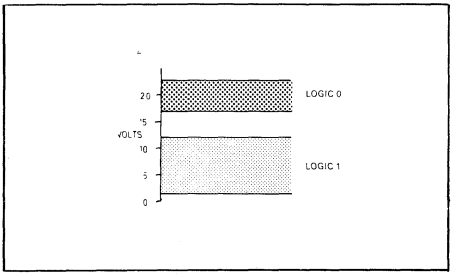


Fig. 4 Worst case DC noise margin: fanout/fanin of 10

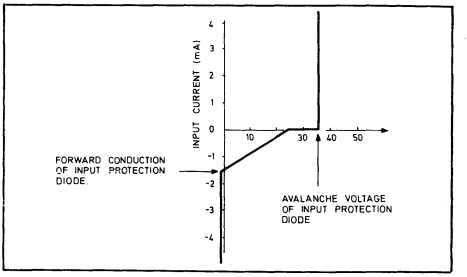


Fig. 5 Typical input characteristic

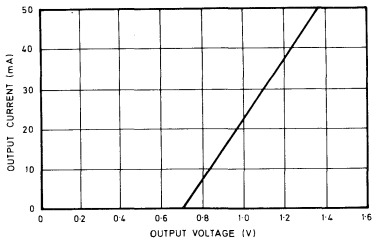


Fig. 6 Typical output characteristic

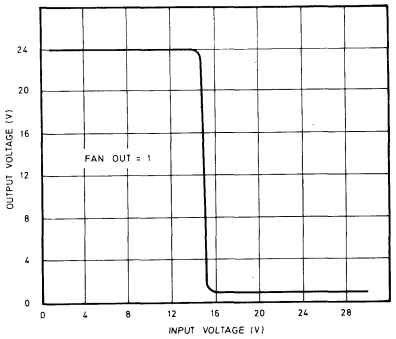


Fig. 7 Typical transfer characteristic for an inverting output: fanout = 1.

OPERATING NOTES

Up to 6 gates may be connected one above the other as shown in Fig.8 to form a wired -AND function. The noise margin will however be reduced to a minimum of 2V. Q1 is capable of driving up to 10 inputs without further reduction of noise margins.

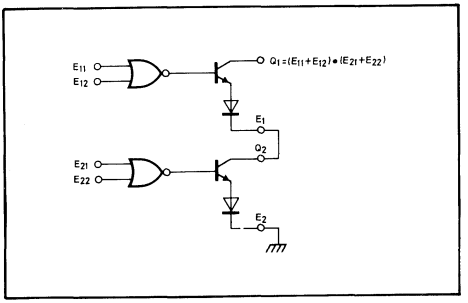


Fig. 8 Wired -AND function

Up to 10 outputs may be connected together as shown in Fig. 9 to form a wired -OR function. The resulting output may fanout to 10 inputs.

A complex gate function may be created by interconnecting several outputs together in both wired -AND and wired -OR configurations to form an array up to 10 outputs in parallel and 6 outputs in series.

By means of an external capacitor inserted as shown in Fig. 10, the output edge transitions may be slowed where this is required.

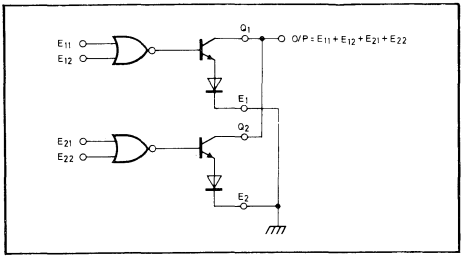


Fig. 9 Wired -OR function

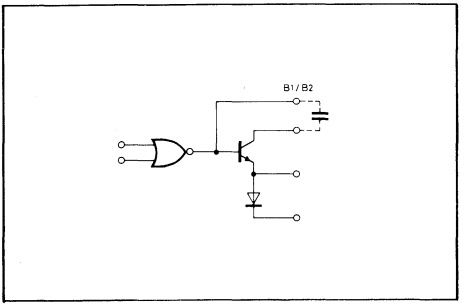


Fig. 10 Outputs B1 and B2

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Operating ambient temperature	−20°C to +70°C
Peak supply surge rating peak for 10ms	90V

PLESSEY
SEMICONDUCTORS

SP530 SERIES
INDUSTRIAL LOGIC

SP532A
COMPLEX LATCH

The SP532, a complex latch, is designed with a persistence detector, its time-out being determined by an external capacitor. This ensures the output does not change state until a logic signal has been present for the pre-determined time. Thus transient noise on a logic input will be ignored and the latch will also maintain its state if there is a transient collapse of the power supply.

With the exception of input A pin, each input is protected from the destructive power of RF noise by a high power avalanche diode connected between the input and 0V. Each input also sources a current in excess of 1mA so a mechanical switch may be reliably used for a logic input. The persistence detector will ensure that there are no contact bounce problems.

True and compliment outputs are provided, each capable of driving 35mA when at a logic 1. The logic 0 is provided by a very high value resistor connected to the internal supply voltage.

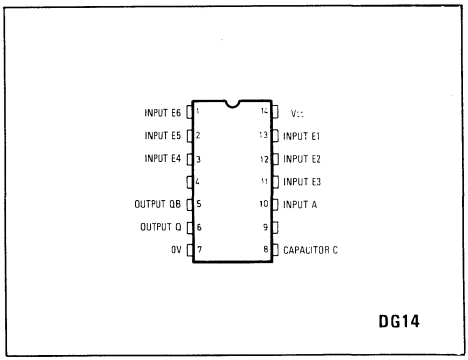


Fig. 1 Pin connections

FEATURES

- Very High Noise Immunity
- Input Protection Against Destructive High Energy Noise Transients
- Ability to Work from Unregulated Poorly Smoothed Power Supply
- Fan In and Fan Out of 10
- Logic Inputs Which Supply Currents for Reliable Use With Mechanical Switches

APPLICATIONS

- Process Control Logic
- Automatic Machine Control
- Logic Circuitry in Telephone Exchanges
- Any Situation where High Noise Levels or High Voltage Requirements Cause Problems for Standard Logic Ranges

QUICK REFERENCE DATA

	Min.	Max.	Units
+Vcc Power Supply Voltage			
Continuous	32	60	V
Transient		90	V
Power Supply Current		19	mA
Open Circuit Input Voltage	22	26	V
Short Circuit Input Current	1	3	mA
Output Saturation Voltage (35mA)		1.6	V
Input Threshold	12	17	V

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = −20°C to +70°C
V_{CC} = 32V to 60V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Static Characteristics					
Power supply drain current			19	mA	V_{in} = 0V all inputs
Inputs E1 – E6					
Open circuit input volts	22		26	V	V_{CC} = 38V–60V
Short circuit input current	1		3	mA	V_{CC} = 38V–60V
Input breakdown voltage	26		55	V	
Input Logic Levels					
Logic 1	−0.4		12	V	
Logic 0	17		26	V	
Input A					
Short circuit input current	0.15		1.0	mA	See note 1
Input A Logic Levels					
Logic 1	0		5	V	
Logic 0	11		26	V	
Output Logic Levels					
Logic 1			1.6	V	I_{OUT} = 35mA
Logic 0 (Leakage)			10	μA	V_{OUT} = 20V
Dynamic Characteristics:					
No external capacitance					
Output rise and fall times 20%–80%			300	μs	Output load:- fan out of 10 in parallel with 500pf
Delay to rise 50% – 50%			300	μs	Input levels: logic 1=12V logic 0=17V
Delay fall 50% – 50%			300	μs	Transition times 10μs
With 0.1 μF external capacitor					
Rise and fall times 20% – 80%			300	μs	
Delay to rise 50% –50%	2.5		5.5	ms	
Delay to fall 50% – 50%	2.5		5.5	ms	

Note 1. Characteristics of A input

This is a 'control' input, intended for hardwiring to a specific logic state; a connection to 0V for a logic 1/and open circuit for a logic 0. No noise protection is therefore provided on this input, and the DC noise margin is greatly reduced.

ABSOLUTE MAXIMUM RATINGS

Storage temperature −55°C to +175°C
Operating ambient temperature −20°C to +70°C
Peak supply surge rating peak for 10ms 90V

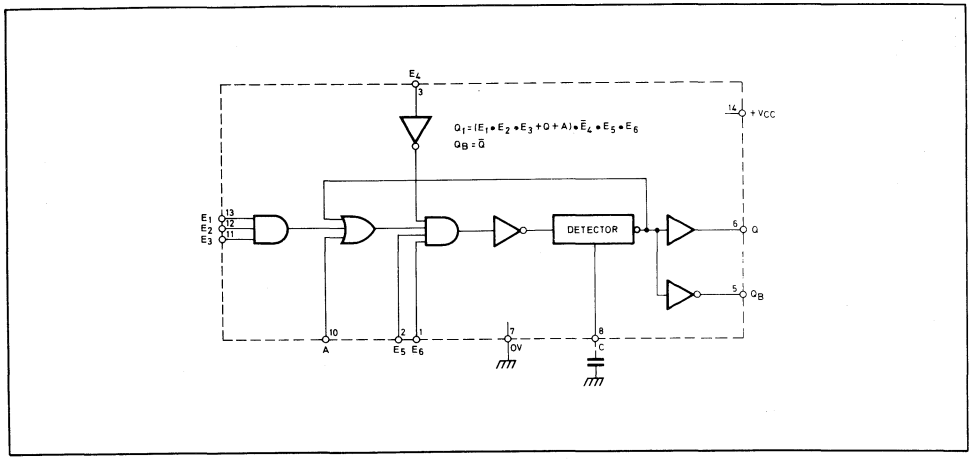


Fig. 2 Functional diagram (negative logic is assumed)

OPERATING NOTES

Up to ten outputs from any of the SP530 logic family may be connected together to form an OR function. One output or up to a 10 wide wired OR output may be used to drive up to 10 inputs.

Initial States After Power On (with capacitor C connected)

After the power on, Output Q will remain at logic 0 (Output Q_B at logic 1) for the duration of the persistence delay; thereafter Output Q will assume the value determined by the inputs.

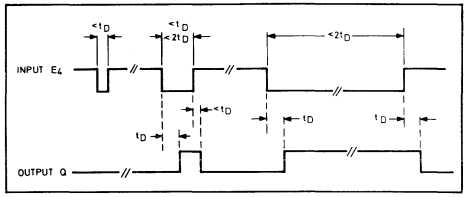


Fig. 3 Timing diagram showing the noise-ignoring effect of the input persistence detector with 0·1uF capacitor. Input E5, E6, A=0V. TD=2·5 to 5·5 ms with 0·1uF capacitor, TD (typical) = 4 x 10⁴ x C, C_{in} Farads T in seconds (valid for T> 500 us)

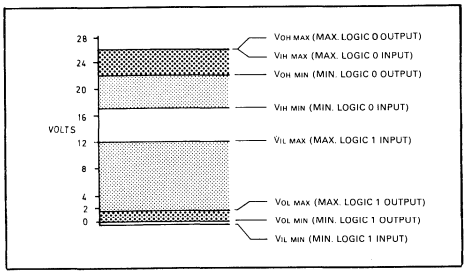


Fig. 4 Logic levels

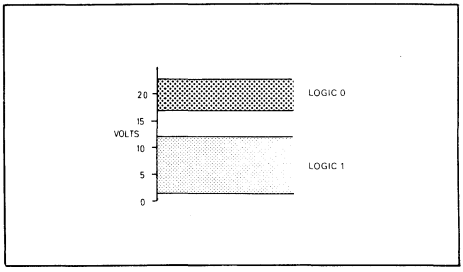


Fig. 5 Worst case DC noise margin: fanout/fan in of 10

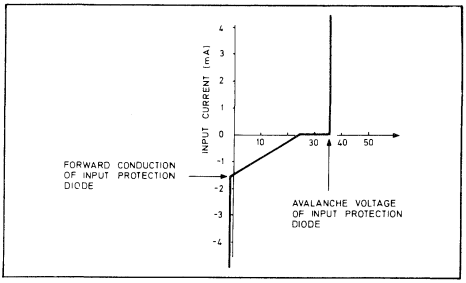


Fig. 6 Typical input characteristic

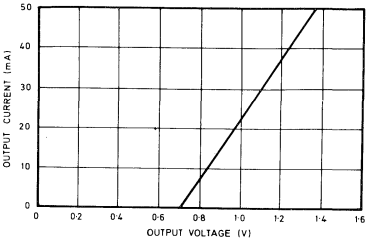


Fig. 7 Typical output characteristic

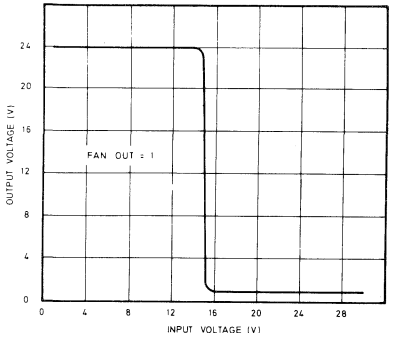


Fig. 8 Typical transfer characteristic for an inverting output: fanout=1

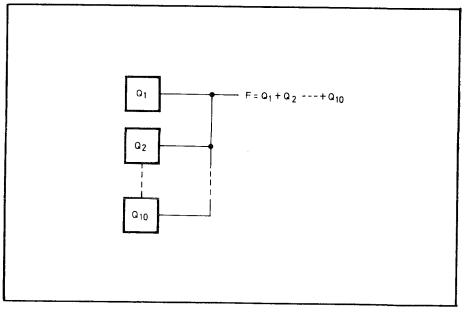


Fig. 9 Wired-OR configuration

PLESSEY
SEMICONDUCTORS

SP530 SERIES
INDUSTRIAL LOGIC

SP533A
VERSATILE TIMING ELEMENT

The SP533 A is a member of a family of high noise immunity industrial logic elements designed for easy use, without the need for external protection, by fabricating the circuitsbon the Plessey High Voltage Process, which has voltage breakdowns in excess of 90V. This process also has a special diffusion for the construction of buried avalanche diodes, which are capable of absorbing powerful noise transients without being destroyed.

The SP533 is an accurate timing element, its period being determined by an external resistor and capacitor. The triggering of the timer is controlled by two inputs. It can be set to be triggered as a delay on either a '0' to '1' or a '1' to '0' logic transition, or as a non-re-triggerable monostable on a '0' to '1' logic transition.

There is a persistance detector on the input, so that the timer is not enabled until an input has been present for a length of time predetermined by another external capacitor. Thus the circuit maintains logical integrity for transients of noise on either the power supply or the input.

Each circuit incorporates its own internal regulated power supply enabling it to work with large variations of voltage and high levels of noise and ripple on the external supply. The logic input is protected from the destructive power of RF noise by a high power avalanche diode connected between the input and ground.

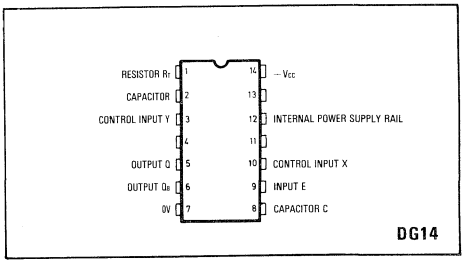


Fig. 1 Pin connections

APPLICATIONS

- Process Control Logic
- Automatic Machine Control
- Logic Circuitry in Telephone Exchanges
- Any Situation where High Noise Levels or High Voltage Requirements Cause Problems for Standard Logic Ranges

FEATURES

- Very High Noise Immunity
- Input Protection Against Destructive High Energy Noise Transients
- Ability to Work from Unregulated Poorly Smoothed Power Supply
- Fan In and Fan Out of 10
- Logic Inputs Which Supply Currents for Reliable Use With Mechanical Switches
- Accurate Timing in a Noisy Environment
- Persistence Detector on Inputs

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Operating ambient temperature	−20°C to +70°C
Peak supply surge rating peak for 10ms	90V

QUICK REFERENCE DATA

	Min.	Max.	Units
+Vcc Power Supply Voltage			
Continuous	32	60	V
Transient		90	V
Open Circuit Input Voltage	22	26	V
Short Circuit Input Current	1	3	mA
Output Saturation Voltage (35mA)		1.6	V
Input Threshold	12	17	V

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = −20°C to +70°C
V_{CC} = 32V to 60V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Static Characteristics					
Power supply drain current			19	mA	V_{in} = 0V all inputs
Inputs E1 – E6					
Open circuit input volts	22		26	V	V_{CC} = 38V–60V
Short circuit input current	1		3	mA	V_{CC} = 38V–60V
Input breakdown voltage	26		55	V	
Input Logic Levels					
Logic 1	−4		12	V	
Logic 0	17		26	V	
Input A					
Short circuit input current	0.15		1.0	mA	See note 1
Input Logic Levels					
Logic 1	0		5	V	
Logic 0	11		26	V	
Output Logic Levels					
Logic 1			1.6	V	I_{OUT} = 35mA
Logic 0 (Leakage)			10	µA	V_{OUT} = 20V
Dynamic Characteristics:					
No external capacitance					
Output rise and fall times 20%–80%			300	µs	Output load:- fan out of 10 in parallel with 500pf
Delay to rise 50% – 50%			300	µs	Input levels: logic 1=12V logic 2=17V
Delay fall 50% – 50%			300	µs	Transition times 10µs
With 0.1 µF external capacitor					
Rise and fall times 20% – 80%			300	µs	
Delay to rise 50% – 80%	2.5		5.5	ms	
Delay to fall 50% – 50%	2.5		5.5	ms	
Timing period					Ambient=25°C T=K.R_T.C_T. RT=100k CT=15 uF
Timing delay constant K	0.68	0.72	0.76		
Temp. coefficient of delay			0.1	%/°C	V_{CC}=48V
Capacitor point (C_T) leakage current			1	µA	
Rearming current	4			mA	

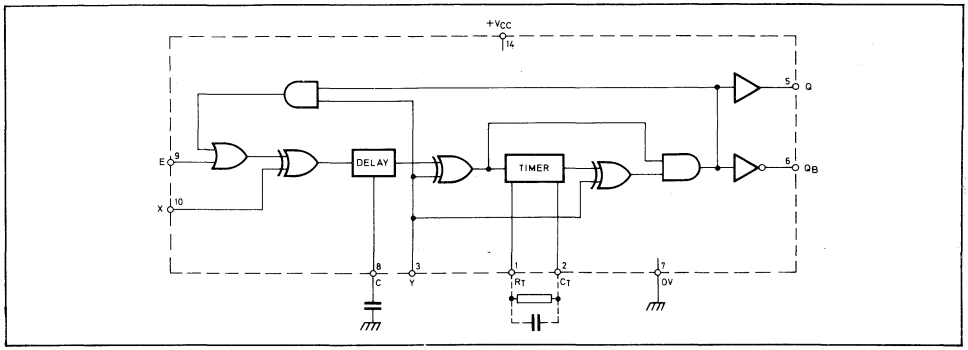


Fig. 2 Functional diagram

OPERATING NOTES

Timing Delay

The length of the timing delay is constant whichever mode the circuit is used in.

Characteristics

The value of the timing period is determined by the following formula:

$T = K C_T R_T$ where K=0.72 typical.

Range of suitable values of R_T=15k R_T 500k

The range of suitable values of capacitance is usually determined by the leakage current of the capacitor. The voltage rating of the capacitor should exceed 25 volts.

Different Circuit Modes

Inputs X and Y are intended for hard wired use, as they have no protection against destruction by noise and have very much lower noise immunity. They may however, bearing the above in mind, be controlled by logic gates.

A logic 1 can be provided by a connection to 0V.

A logic 0 can be provided be either a connection to V_{INT} or left open circuit.

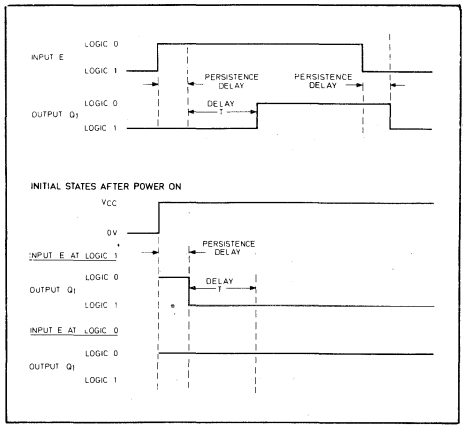


Fig. 3 Reset delay Control input X at logic '1'. Control input Y at logic '0'. Capacitor C_T connected between pin 1 and pin 2. Persistence delay capacitor C and resistor R_T connected as function diagram.

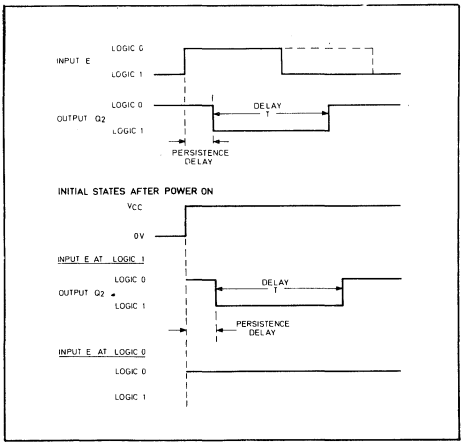


Fig. 4 Different configuration, true outputs only. Control inputs X and Y at logic '0'. Capacitor C_T connected between Pin 2 and 0V. Persistence delay capacitor C and resistor R_T connected as function diagram.

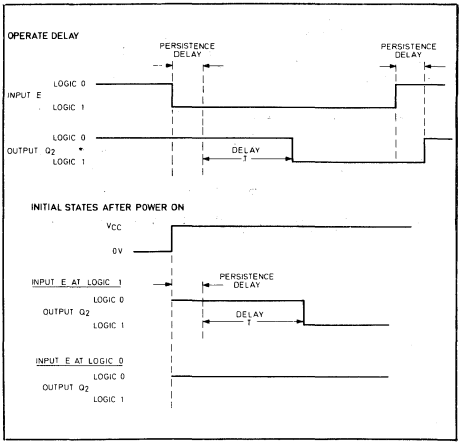


Fig. 5 Non-retriggerable monostable

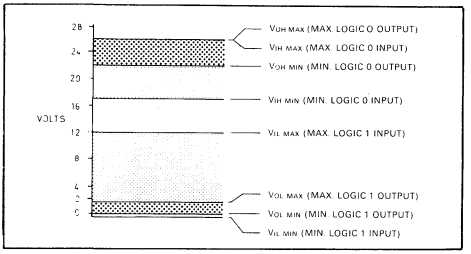


Fig. 6 Logic levels

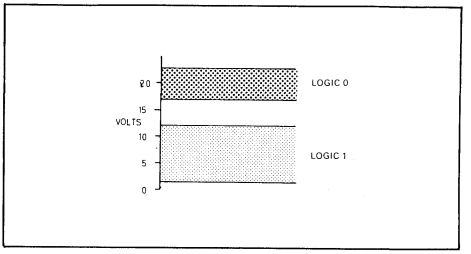


Fig. 7 Worst case DC noise margin: fanout/fan in of 10

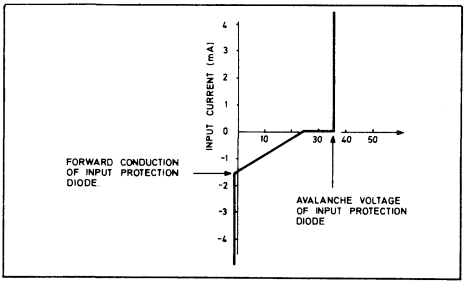


Fig. 8 Typical input characteristic

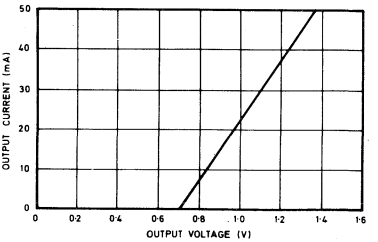


Fig. 9 Typical output characteristic

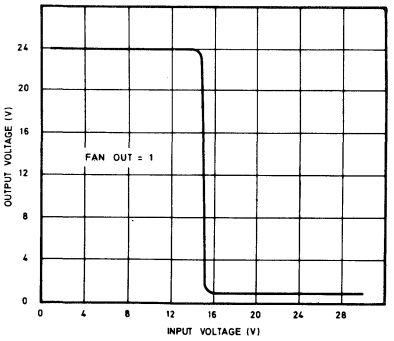


Fig. 10 Typical transfer characteristic for an inverting output: fanout=1

PLESSEY
SEMICONDUCTORS

SP530 SERIES
INDUSTRIAL LOGIC

SP534A
COMPLEX GATE

The SP534 is a member of a family of high noise. immunity industrial logic elements designed for easy use, without the need for external protection, by fabricating the circuitsbon the Plessey High Voltage Process, which has voltage breakdowns in excess of 90V. This process also has a special diffusion for the construction of buried avalanche diodes, which are capable of absorbing powerful noise transients without being destroyed.

The SP534, a complex gate, is designed with a persistence detector, its time-out being determined by an external capacitor. This ensures the output does not change state until a logic signal has been present for the pre-determined time. Thus transient noise on a logic input will be ignored and the latch will also maintain its state if there is a transient collapse of the power supply.

Each circuit incorporates its own internal, regulated power supply, enabling it to work with large variations of voltage and high levels of noise and ripple on the external supply.

With the exception of input A pin, each input is protected from the destructive power of RF noise by a high power avalanche diode connected between the input and 0V. Each input also sources a current in excess of 1mA so a mechanical switch may be reliably used for a logic input. The persistence detector will ensure that there are no contact bounce problems.

True and compliment outputs are provided, each capable of driving 35mA when at a logic 1. The logic 0 is provided by a very high value resistor connected to the internal supply voltage.

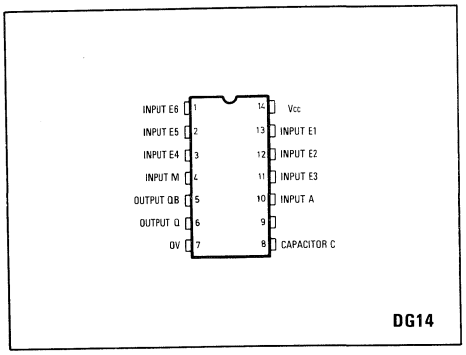


Fig. 1 Pin connections (top)

APPLICATIONS

- Process Control Logic
- Automatic Machine Control
- Logic Circuitry in Telephone Exchanges
- Any Situation where High Noise Levels or High Voltage Requirements Cause Problems for Standard Logic Ranges

QUICK REFERENCE DATA

	Min.	Max.	Units
+Vcc Power Supply Voltage			
Continuous	32	60	V
Transient		90V	
Power Supply Current		15	mA
Open Circuit Input Voltage	22	26	V
Short Circuit Input Current	1	3	mA
Output Saturation Voltage (35mA)		1.6	V
Input Threshold	12	17	V

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Operating ambient temperature	−20°C to −70°C
Peak supply surge rating peak for 10ms	90V

FEATURES

- Very High Noise Immunity
- Input Protection Against Destructive High Energy Noise Transients
- Ability to Work from Unregulated Poorly Smoothed Power Supply
- Fan In and Fan Out of 10
- Logic Inputs Which Supply Currents for Reliable Use With Mechanical Switches

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = −20°C to +70°C
V_{CC} = 32V to 60V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Static Characteristics					
Power supply drain current			19	mA	V_{in} = 0V all inputs
Inputs E1 – E6					
Open circuit input volts	22		26	V	V_{CC} = 38V–60V
Short circuit input current	1		3	mA	V_{CC} = 38V–60V
Input breakdown voltage	26		55	V	
Input Logic Levels					
Logic 1	– 4		12	V	
Logic 0	17		26	V	
Input A					
Short circuit input current	0.15		1.0	mA	See note 1
Input Logic Levels					
Logic 1	0		5	V	
Logic 0	11		26	V	
Output Logic Levels					
Logic 1			1.6	V	I_{OUT} = 35mA
Logic 0 (Leakage)			10	μA	V_{OUT} = 20V
Dynamic Characteristics:					
No external capacitance					
Output rise and fall times 20%–80%			300	μs	Output load :- fan out of 10 in parallel with 500pf
Delay to rise 50% – 50%			300	μs	Input levels: logic 1=12V logic 2=17V
Delay fall 50% – 50%			300	μs	Transition times 10μs
With 0.1 μF external capacitor					
Rise and fall times 20% – 80%			300	μs	
Delay to rise 50% – 50%	2.5		5.5	ms	
Delay to fall 50% – 50%	2.5		5.5	ms	

Note 1. Characteristics of A input

This is a 'control' input, intended for hardwiring to a specific logic state; a connection to 0V for a logic 1/and open circuit for a logic 0. No noise protection is therefore provided on this input, and the DC noise margin is greatly reduced.

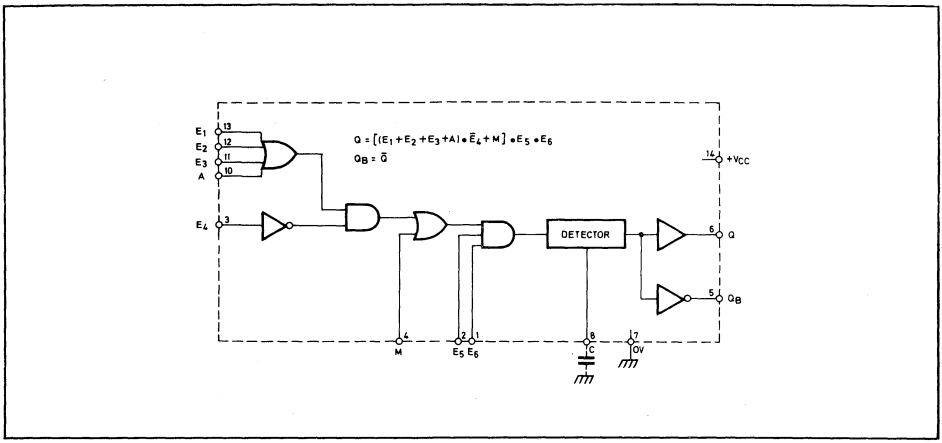


Fig. 2 Functional diagram (negative logic)

OPERATING NOTES

Up to ten outputs from any of the SP530 logic family may be connected together to form an OR function. One output or up to a 10 wide wired OR output may be used to drive up to 10 inputs.

Initial States After Power On (with capacitor C connected)

After the power on, Output Q will remain at logic 0 (Output Q_B at logic 1) for the duration of the persistence delay; thereafter Output Q will assume the value determined by the inputs.

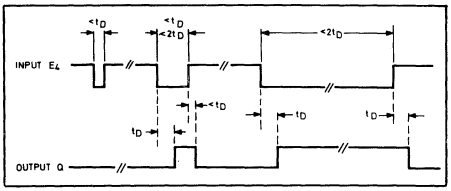


Fig. 3 Timing diagram showing the noise-ignoring effect of the input persistence detector with 0·1uF capacitor. Input E5, E6, A=0V, TD=2·5 to 5·5 ms with 0·1uF capacitor, TD (typical) = 4 x 10⁴ x C, C_{in} Farads T in seconds (valid for T> 500 us)

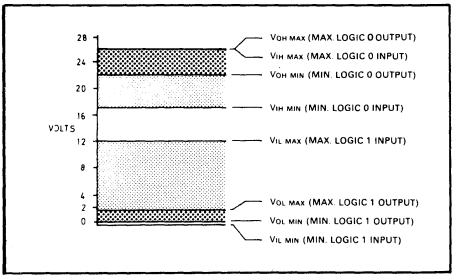


Fig. 4 Logic levels

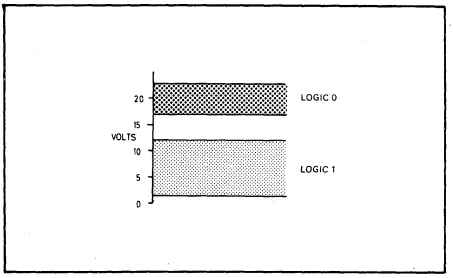


Fig. 5 Worst case DC noise margin: fanout/fan in of 10

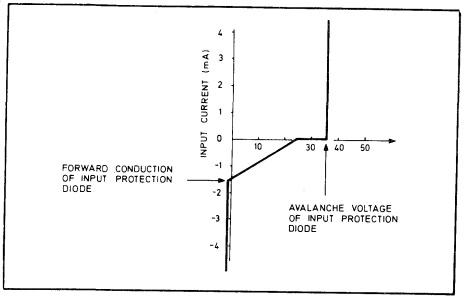


Fig. 6 Typical input characteristic

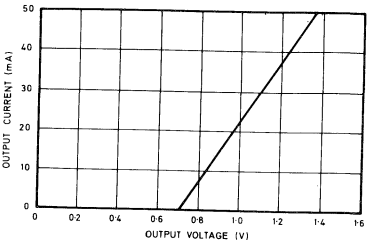


Fig. 7 Typical output characteristic

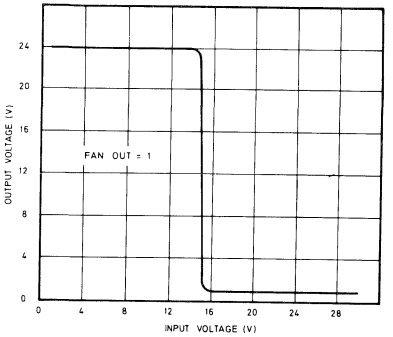


Fig. 8 Typical transfer characteristic for an inverting output: fanout=1

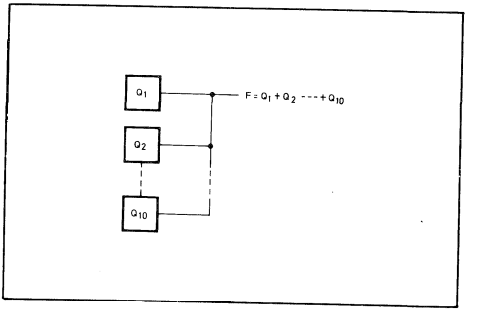


Fig. 9 Wired-OR configuration

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

SP701A TTL-MOS ANALOGUE SWITCH DRIVER
SP703A TTL-MOS ANALOGUE SWITCH AND LOGIC DRIVER
SP704A TTL-MOS ANALOGUE SWITCH AND LOGIC DRIVER

The SP701, SP703 and SP704 are bipolar integrated circuits designed to accept the output swing from saturating bipolar logic such as RTL, DTL and TTL, and provide outputs suitable for driving MOS devices. The SP704 differs from the other devices in the range in that it has one voltage input and a current input designed to accept the output from MOS logic. The SP701 is available in 10-lead TO-5, while the SP703 and SP704 are packaged in 14-lead ceramic DIL.

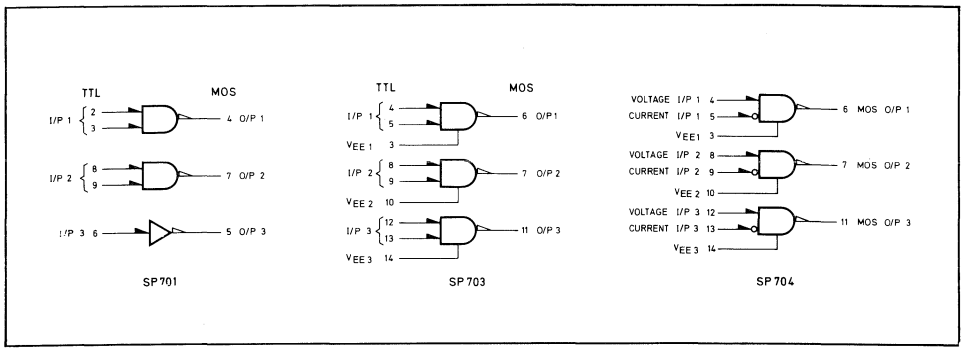


Fig. 1 Logic and package connection diagrams

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance (TO-5)	250°C/W
Chip-to-case thermal resistance (TO-5)	80°C/W
Chip-to-ambient thermal resistance (dual-in-line)	150°C/W
Total supply voltage (Vs) (Vcc with respect to VEE; or Vcc, strapped to 0V, with respect to VEE on SP703 and SP704)	
All types except SP703B	30V
SP703B	20V
Input voltage relative to Vcc (voltage inputs)	0 to —7V
Mean input current (current inputs on SP704)	20mA
Mean output current	—10mA to +10mA

It is necessary to use a heat sink if the junction temperature - calculated from the maximum ambient temperature and the maximum power dissipation - would otherwise exceed +175°C.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 0 C to 70 C
All voltages are measured with respect to V_{CC}
Output 'high' means nearest V_{CC} or 0V; output 'low' means nearest V_{EE}
Current convention: positive current that is flowing into the device.

Characteristic	Circuit	Value			Units	Test conditions
		Min.	Typ.	Max.		
Input and output levels						
I/P voltage for)/P 'low'	All types except SP704 current I/Ps			0.8	V(neg.)	
I/P current for O/P 'low'	SP704 current I/Ps			50	μA(pos.)	Voltage I/Ps to V_{CC}
I/P voltage for O/P 'high'	All types except SP704 current I/Ps	2.75			V(neg.)	
I/P current for O/P 'high'	SP704 voltage I/Ps			1.0	mA(neg.)	V_{in}=—2.75V
" "	SP704 current I/Ps	400			μA(pos.)	
O/P 'high' voltage with respect to V_{CC}	SP701	0	0.7	1.2	V(neg.)	No load current
" "		5	6	7	V(neg.)	No load current
O/P 'high' voltage with respect to OV	SP703A, B & SP704A,	0	0.7	1.2	V(neg.)	No load current
O/P 'low' voltage with respect to V_{EE}	All types		0.8	1.5	V(pos.)	No load current
Power consumption						
Power consumption per circuit with O/P 'high' (Note 1)	SP701A		43	60	mW	V_{in}=—2.75V V_S=20V
" "	SP701A		60	80	mW	V_{in}=—2.75V V_S=25V
" "	SP701A,		80	110	mW	V_{in}=—2.75V V_S=30V
" "	SP703A & SP704A		32	43	mW	V_{CC}= -5V, V_S=20V
" "	SP703A & SP704A		45	60	mW	V_{CC}= -5V, V_S=25V
" "	SP703A & SP704A		60	80	mW	V_{CC}= -5V, V_S=30V (If V_{CC} is strapped to 0V, power consumption is as for SP701A & SP702A).
Power consumption per circuit with O/P 'low'	SP701A		60	80	mW	V_S=20V
" "	SP701A		90	120	mW	V_S=25V V_{in}=—0.8V
" "	SP701A		120	160	mW	V_S=30V
Power consumption per circuit with O/P 'low'	SP703A, & SP704A		40	55	mW	V_S=20V
" "	SP703A & SP704A		66	90	mW	V_S=25V V_{in}=—0.8V V_{CC}= +5V
" "	SP703A & SP704A		100	135	mW	V_S=30V (If V_{CC} is strapped to 0V, power consumption is as for SP701A and SP702A)
Switching times (Note 2)						
Turn-on delay t_{di}	All types		25		nS	C_L=10pF
" "	"		30		nS	C_L=100pF
Turn-on rise time t_r	"		25		nS	C_L=10pF
" "	"		75		nS	C_L=100pF
Turn-off delay t_{d2}	"		30		nS	C_L=10pF
" "	"		35		nS	C_L=100pF
Turn-off fall time t_f	"		30		nS	C_L=10pF
" "	"		65		nS	C_L=100pF

NOTES
1. The figures quoted apply to the 'no load' condition and are suitable for calculating the total power consumption when driving capacitive loads at repetition rates below 10kHz.
2. These switching times are applicable to the current inputs of the SP704A provided that drive currents are < 50uA for turn-on and > 400μA for turn-off.

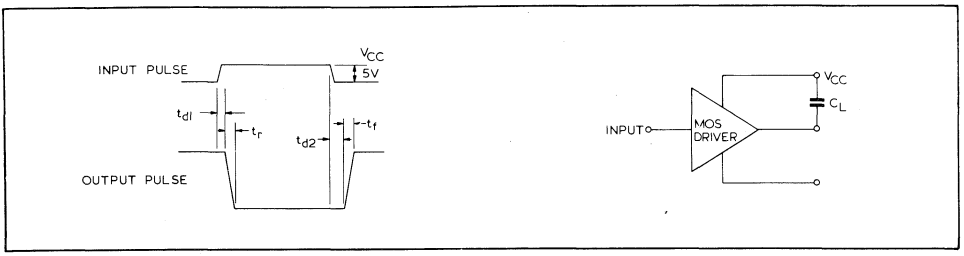


Fig. 2 Switching times

OPERATING NOTES

These circuits can be driven from almost any standard logic family. With low or medium-power RTL, no logic fan-out can be permitted for the RTL element other than the connection to the MOS driver; the extra current drawn from the MOS driver input requires that the RTL driving gate fan-out be taken as 2.

Where the driven MOS device incorporates gate protection, its gate protection diode will be forward biased whenever the gate voltage exceeds the substrate voltage by one diode drop. The SP701 outputs are optimised for driving MOS analogue switches, which have substrate connected to VCC.

The greater flexibility of application of the SP703 and SP704 results from the use of separate supply rails for input and output circuits. In addition, the three circuits of the SP703 and SP704 have separate VEE rails which may be operated at different voltages provided that VEE3 (pin 14) is the most negative.

One of the two inputs to each gate in the SP704 is a current input designed to be driven from MOS logic; the SP704 may thus be used as a high fan-out buffer element in MOS logic systems.

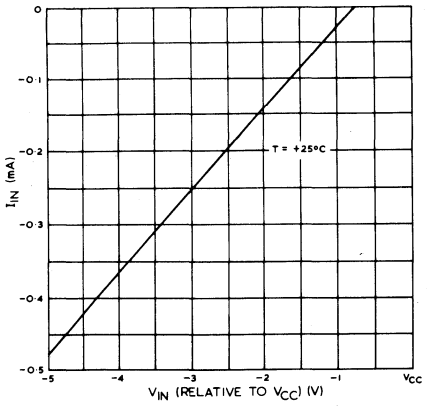


Fig. 3 Typical input characteristics

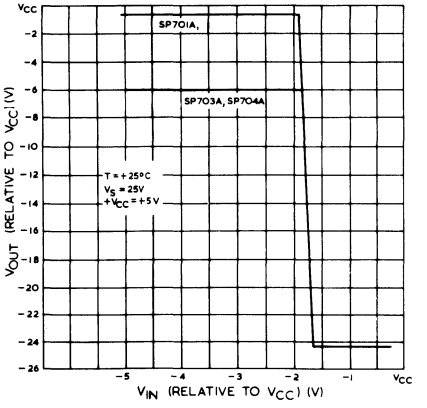


Fig. 4 Typical voltage transfer characteristics

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

SP705B
CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: $f/2$, $f/4$, $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications

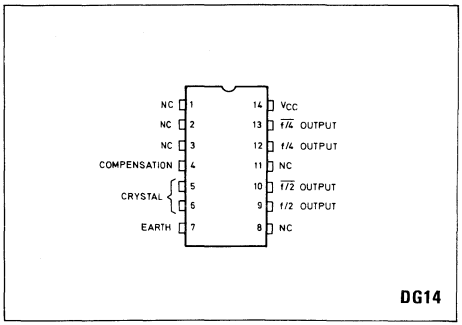


Fig.1 Pin connections

FEATURES

- Operating Frequency up to 10 MHz
- $f/2$ and $f/4$ outputs
- 4 TTL Level outputs
- Operates from +5V TTL Supply

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	V_{OH}	2.6		V	V_{CC} = 4.75V I_{OH} = 0.2 mA
Low state output voltage	V_{OL}		0.4	V	V_{CC} = 5.25V I_{OL} = 8 mA
Supply current	I_{CC}		35	mA	V_{CC} = 5V
Output rise time (10% to 90%)	t_R		20	ns	V_{CC} = 5V
Output fall time (90% to 10%)	t_F		20	ns	V_{CC} = 5V
Operating frequency (f)			10	MHz	
Operating temp range		0	70	°C	

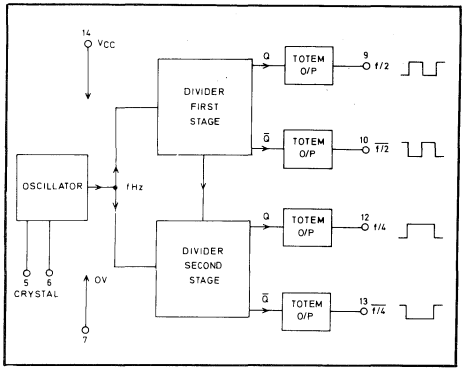


Fig. 2 SP705B block diagram

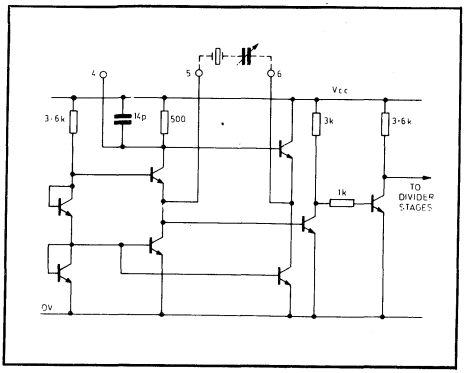


Fig. 3 Circuit diagram of SP705B oscillator

CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig. 3.

The circuit is designed to provide low crystal drive levels – typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

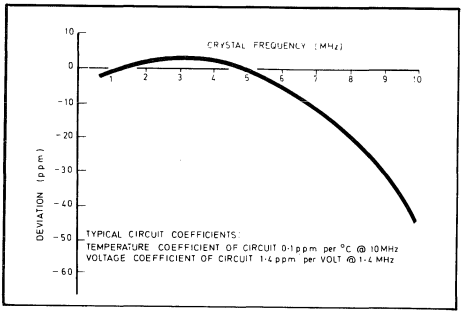


Fig. 4 Deviation from nominal crystal frequency

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

SP721B BALANCED LINE DRIVER
SP722B BALANCED LINE RECEIVER
SP724B DUAL BALANCED LINE RECEIVER

The SP721B, SP722B and SP724B circuits are designed for interfacing between TTL/DTL logic and balanced transmission lines. The SP721B line driver produces an output which is essentially a current sink into one of the two lines. The magnitude of the current is nominally twice that of an externally programmed source current. The receiver circuits will accept anti-phase signals from a line with a DC level several volts remote from earth potential.

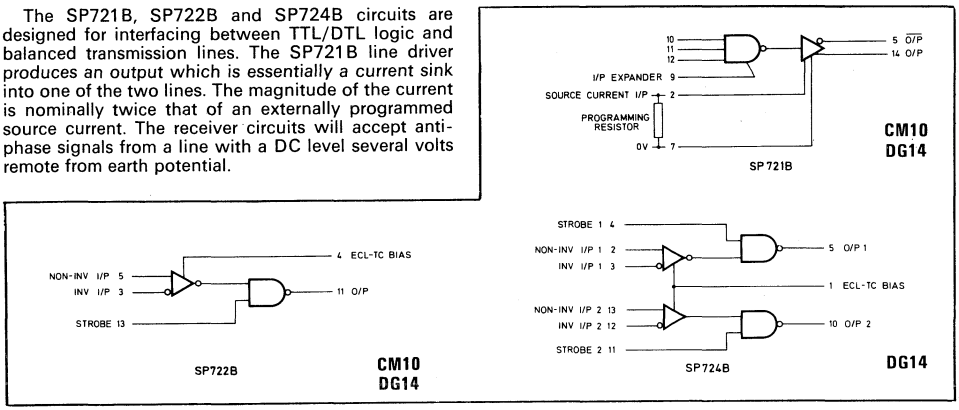


Fig. 1 Logic diagrams. Note: pin numbers are identical for all packages.

OPERATING NOTES

The SP721B Balanced line driver, accepts TTL logic inputs, and its output to line is in the form of a differential current sink. The current flows from the line into one of the two output terminals, setting up a differential voltage on the line. The magnitude of this current sink is determined by the value of external programming resistor between pins 7 and 2 and is nominally twice the current flowing into pin 2. The size of the differential voltage produced on the line, is dependent on the current chosen and the differential impedance of the line.

A recommended standard is 8mA (minimum) into a 100 Ω line giving an 800mV differential signal.

The line receivers will accept up to a 3V common mode input without being affected, responding only to differential signals producing TTL compatible outputs.

Point to Point Working

Fig. 3 shows a typical configuration with balanced matched lines terminated at both ends. It is possible to match only the differential impedance, but problems may arise from reflected common mode signals which may then exceed the 3V limit. To overcome this problem, the network shown gives a common mode termination of about 60 Ω corresponding to a typical screened sheath pair cable. Using low loss cable in this way, signals can be transmitted a distance of at least 150 metres, at clock rates up to 5 MHz.

The common mode line figure of 3V can be improved by attenuating the cable signals to the receiver, at the expense of differential sensitivity. Typically an attenuation up to 5 times (14 dB) may be used before the differential error becomes excessive.

When more than one receiver or transmitter are used it is important that all transmitters and receivers connected to a line are always connected to common power supplies.

Distribution of Multiple Receivers

Each receiver has only a small disturbing influence, so several receivers may be connected on to one line at different points. However it is possible that common mode problems may be accentuated, so it is often advisable to carry out attenuation as suggested in the paragraph on point to point working.

Multiple Transmitters for Highway Working

By strobing the programming current supplied to pin 2 of the SP721B, the output from that transmitter can be switched on or off. This however produces a large common mode shock which takes time to decay, the decay time depending on the line length and line characteristics. Thus the SP721B can be used for block data transfer, provided sufficient time is allowed between blocks, for the common mode shocks to decay.

ELECTRICAL CHARACTERISTICS (SP721B)

Test conditions (unless otherwise stated):
$V_{CC} = -5V \pm 5\%$
$V_{EE} = -5V \pm 5\%$
$T = 0°$ to 70 C

Characteristic	Value			Units	Test conditions
	Min.	Typ.	Max.		
Input voltage for logic '0' O/P	0		800	mV	—
Input current for logic '0' O/P			1.6	mA (neg.)	$V_{IN} = 0.4V$
Input voltage for logic '1' O/P	2.0			V	—
Input current for logic '1' O/P			40	μA	$V_{IN} = 2.4V$
Output current at pin 5 for logic '0' O/P			1.0	μA	
Output current at pin 14 for logic '0' O/P	1.4	2.0	2.6	/unit source current	Note 1
Output current at pin 14 for logic '1' O/P			1.0	μA	Note 1
Output current at pin 5 for logic '1' O/P	1.4	2.0	2.6	/unit source current	Note 1
Output current difference between logic '0' and logic '1'			100	μA	Note 1
Permissible output voltage excursion	—3		+3	V	Notes 1 and 2
Mean propagation delay (tpu − tpd)/2		15		nS	Note 3
Propagation delay skew			5	nS	Note 4
Dissipation		150	260	mW	Note 5
Supply current (+5V)		5.5	7.0	mA	$I_{SOURCE} = 10mA$
Supply current (—5V)		33	45	mA	

NOTES (D.I.L. pins quoted)

1. This result holds for the source current in the range 1 to 10mA (pin 2) and this current is normally determined by a resistor from pin 2 to ground (see fig. 2).

2. The voltage indicated is an absolute voltage and to determine the common mode value, the signal voltage must be subtracted from the absolute voltage. The maximum signal voltage = 2.6 x source current x effective load resistor.

3. The time period measured, is from the time when the input passes through the threshold of the circuit, until the output currents at pins 14 and 5, are equal.

4. The propagation delay skew is the time for which the sum of the current at pins 14 and 5 differs from the d.c. value by more than 50% on switching the output state.

5. A duty cycle of 50% is assumed, but if the output is permanently in the logic '1' state the dissipation will be 10mW higher. The source current is set at 10mA.

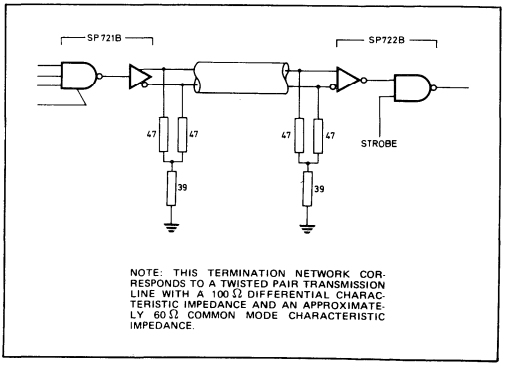


Fig. 2 Typical application.

ELECTRICAL CHARACTERISTICS (SP722B & SP724B)

Test conditions (unless otherwise stated):
V_{CC} = +5V ±5%
V_{EE} = −5V ±5%
T = 0° to 70°C

Characteristic	Circuit	Value			Units	Test conditions
		Min.	Typ.	Max.		
Input voltage (common mode)	All	−3	0	+3	V	—
Input offset	SP722		4.5	15	mV	V_{OUT} = 1.5V
	SP724	5	10	15	mV	V_{OUT} = 1.5V
Input threshold	All		4.5		mV	Note 1
Input current	All			100	µA	—
Input capacitance	All		1	2	pF	Note 2
Input current for logic '0' I/P	All			1.6	mA (neg.)	V_{IN} = 0.4V
Input current for logic '1' I/P	All			120	µA	V_{IN} = 2.4V
Output voltage for logic '0' O/P	All			400	mV	I_O = 0 to 16mA
Output voltage for logic '1' /OP	All	2.4			V	I_O = 0 to 400µA
Mean propagation delay	All		20		nS	—
Dissipation	SP722			145	mW	—
	SP724		170	230	mW	—
Short circuit output current	All	18		55	mA	Note 3
Supply current (+5V)	SP722		12	16	mA	—
	SP724		19	27	mA	—
Supply current (−5V)	All		9	12.5	mA	—

NOTES
1. Measured from offset to give full logic '0' or logic '1' at output.
2. As input passes through threshold, capacitance temporarily rises to 10pF.
3. Not more than one output should be shorted at any one time. This parameter is measured at the maximum recommended supply voltage.

ABSOLUTE MAXIMUM RATINGS
(all devices unless otherwise stated)

Storage temperature range −55°C to +175°C
Operating temperature range 0°C to + 70°C
Dissipation (at T_{amb} = 70°C)
(SP721B) 300mW
Positive supply +6.5V
Negative supply −6.5V
Logic input excursion +5V to −0.5V
Line input excursion (receivers) ±5, or power supply rail values, whichever are the lower
Line output excursion (SP721B) +5V to neg. supply
Line output excursion (SP721B) +5V to neg. supply
Line input differential voltage (receivers) 6V
Source current input (SP721B) 20mA

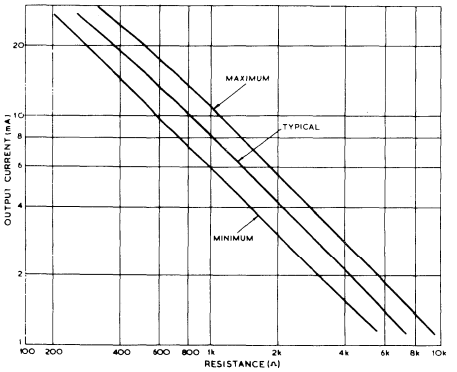


Fig. 3 Output current v. resistance between pin 2 and 0V, assuming 5% tolerance on resistance.

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

SP750B
HIGH SPEED COMPARATOR

The SP750B is a high speed comparator with a latch circuit and other facilities intended for use in the construction of ultra fast A-D converter systems. The speed capability of the device is compatible with conversion rates of up to 100 Mega samples per second. Input and output logic levels are ECL compatible.

FEATURES

- Minimum Set-up Time 2 ns
- Max. Input Offset Voltage 5 mV
- Propagation Delay 3.5 ns
- ECL Compatible
- Comparator Output Gating
- Wired OR Decoding for 4 Bits
- Precision Current Output

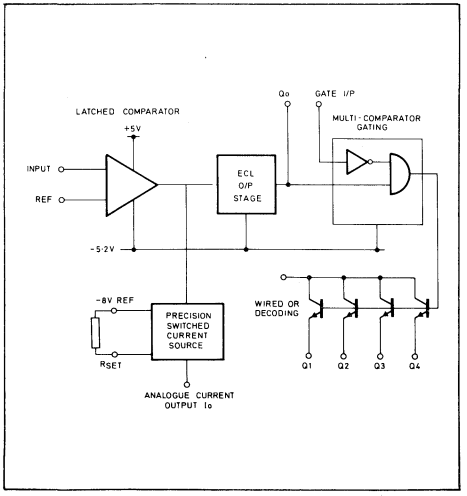


Fig. 2 SP750B schematic diagram

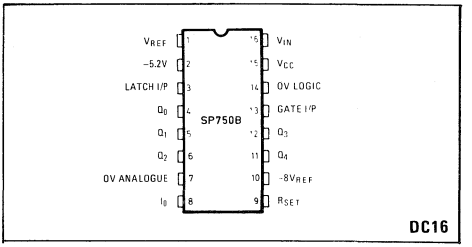


Fig. 1 Pin connections

GENERAL DESCRIPTION

The basis of the SP750B is a fast comparator with a combined latch facility, which allows the comparator to be operated in the hold mode. The comparator has a relatively low gain in the follow mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch facility, the gain approaches infinity during the latch cycle, thereby permitting high resolution.

In addition to the basic comparator, the following functions are provided on the chip. to optimise the performance of high speed parallel-series-parallel A to D converter systems.

1. A two-input gate for simplified multi-comparator output logic.
2. Four emitter follower outputs from the gate to provide wired OR decoding for four bits.
3. A precision current source, set by an external resistor.
4. A high speed switch for the precision current to provide a fast and convenient reconstruction of the analogue input. Summing the currents in a multi-level comparator chain provides the D to A conversion directly for the construction of converters, of the parallel-series-parallel (or feed forward) type.

The philosophy adopted in the SP750B makes possible the construction of ultra fast high accuracy feed forward converters by integrating a significant proportion of the system function on the same chip as the comparator. The result is not only to reduce considerably the total hardware count but to reduce the propagation delays where they are most critical, and eliminate redundant operations.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage			5	mV	
Input bias current			25	μA	
Input offset current			5	μA	
Supply currents					
+5V		16		mA	
−5.2V		35		mA	
−8V		15		mA	
Total power dissipation			470	mW	
Analogue O/P current (I_o) ON		5		mA	See note 1
Anologue O/P current (I_o)			5	μA	
Precision current stability		20		ppm/°C	
Min. latch set-up time			2	ns	See note 2
Input to Q_o O/P delay		3.5		ns	V_{IN} = 100 mV, 25 mV overdrive (see note 3)
Input to I_o delay		3.5		ns	V_{IN} = 100 mV, 25 mV overdrive (see note 3)
Gate delay I/P to Q_{1-4} high		1.6		ns	
Gate delay I/P to Q_{1-4} low		1.3		ns	
Latch enable to I_o between 50% points		2		ns	
Latch enable to I_o, to settle within 0.2%		10		ns	
Minimum hold time		1		ns	
Minimum latch pulse width		2		ns	
Common mode range		±1.5		V	

NOTES
1. The analogue output current (I_o) is set by means of an external setting resistor (R_{set}) and is equal to the reference voltage on Pin 9 (−8V nominal), divided by 2 x R_{set}. Naturally the accuracy of this reference voltage must be consistent with the conversion accuracy required. The allowable voltage on the current output Pin 8, is −8V to +5V.
2. This parameter is measured with +100 mV input and −5mV overdrive, corrected to take account of the comparator offset, i.e. the switching threshold is at 0 V on the input waveform. The minimum set up time is defined as the minimum delay between the time the input voltage crosses the input offset voltage to the 50% crossing of the latch input, required to latch the Q_o output into the correct state. (See Figures 3 and 4). When the latch is low the comparator is in the "follow" mode, and when the latch is driven high the latch locks the output in the existing state.
3. Due to the relatively low gain of the comparator, propagation measurements in the "follow" mode (i.e. not using a latch input), are made with a 25 mV overdrive rather than a 5 mV overdrive.

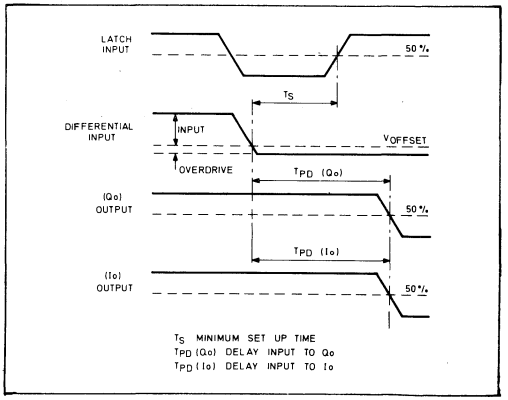


Fig. 3 Timing waveforms

MEASUREMENT OF DYNAMIC PERFORMANCE PERFORMANCE

The accepted standard method of testing the speed performance of a comparator is to apply a 100 mV input step with a 5 mV overdrive level. The 100 mV turns the input stage hard on whilst the 5 mV is more than sufficient to drive the output over the centre of its range. This technique exercises both the large and small signal responses of the comparator, and therefore gives a good measure of the worst case performance of the device under test, whilst avoiding undue difficulties in test pulse generation. (Larger pulses with small overdrives would require extreme purity of waveform.) Minimum set-up time and propagation delay are measured from the time the input signal crosses the input threshold, i.e. the input offset voltage.

The test arrangement shown in Fig. 4 provides automatic correction for the input offset voltage by means of a feedback loop. An input signal referred to earth (0V) may therefore be used, thereby simplifying test pulse generation.

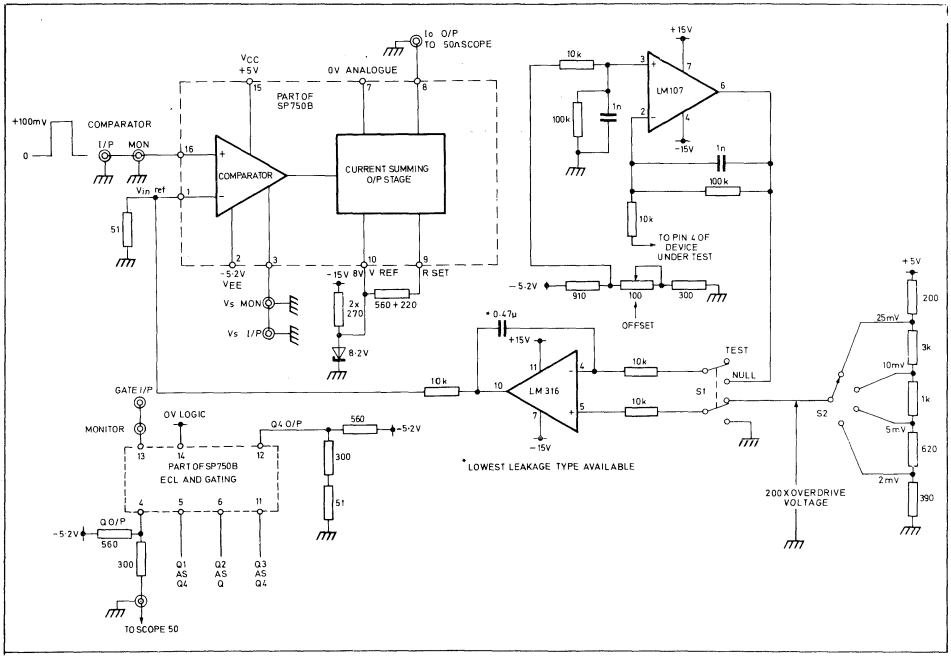


Fig. 4 Dynamic test circuit

In the above circuit, with S1 switched to NULL the feedback corrects the offset in the circuit including DC errors in the 0V level of the input pulse. In the test position, the offset is stored in the integrator capacitor C. Switch S2 adds an overdrive voltage which is selectable. The input duty cycle is made very short so that it does not contribute a significant DC offset.

APPLICATIONS

Although the SP750B was aimed at a particular system configuration, it is sufficiently flexible to find application in a variety of conversion methods.

In an all-parallel A-D converter the SP750B is capable of achieving sampling rates of up to 100 Megasamples per second. This technique is usable up to 5-bit accuracy. An arrangement similar to that shown in Fig. 5 is suitable for this type of converter.

For higher bit accuracies, techniques such as the parallel-series method are required. Fig. 5 shows the schematic diagram of an A-D converter system capable of giving 8-bit accuracy at sampling rates of up to 30 Megasamples per second. The SP750B is used in two 4-bit stages operating in the parallel-series-parallel method of conversion. Full use is made of the wired OR decoding and the analogue output current. Fig. 6 shows a 4-bit stage in greater detail.

In order to achieve the optimum performance of this device, care must be taken to ensure that a good layout is used, consistent with all high frequency practices. A ground plane construction should be used and all leads which are not designed to be microstrip transmission lines should be kept as short as possible. The device should be soldered directly into the circuit board and the supplies should be well decoupled with RF capacitors close to the device. In addition, to achieve the shortest settling time for the analogue current output, it is essential to keep the stray capacitance on Pin 9 (R_{set}) to a minimum.

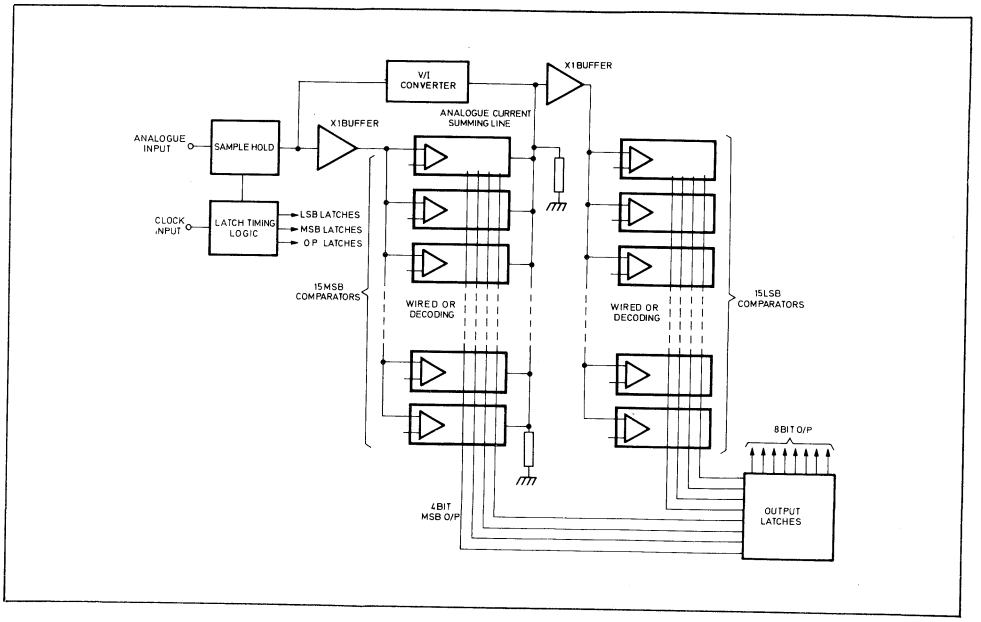


Fig.5 Block diagram of a 4 x 4 bit parallel-series A/D converter

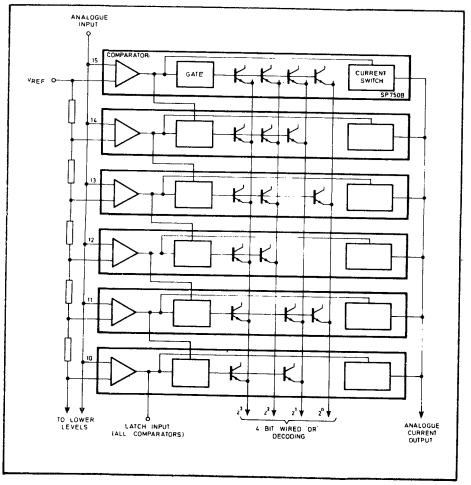


Fig. 6 Block diagram of 4-bit LSB stage showing top six levels

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

SP761B 12V POWER INTERFACE CIRCUIT
SP762B 5V POWER INTERFACE CIRCUIT

The SP761B and SP762B are bipolar integrated circuits, each incorporating five current amplifiers for interfacing between MOS/TTL devices and loads requiring high drive currents. The SP761B is designed to operate from a +12V supply rail and the SP762B from +5V.

Both types are provided with a strobe input which drives two of the amplifiers so that their outputs may be connected in parallel for higher output current capability.

The circuits operate over a temperature range of 0°C to +70°C and are mounted in 14-lead ceramic DIL package.

Although primarily designed to drive printing solenoids in calculators, these circuits can be used in a variety of applications requiring high drive currents.

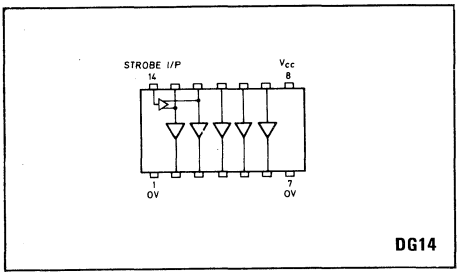


Fig. 1 Pin connections (top)

FEATURES

- Input – MOS/TTL Capability
- Output – 200 mA Capability
- Five Channels per Package
- Open Collector Output

APPLICATIONS

- Driving Solenoids
- Driving Relays
- Driving LEDs
- Driving Filament Lamps
- Driving Cores
- TTL-to-MOS Translator

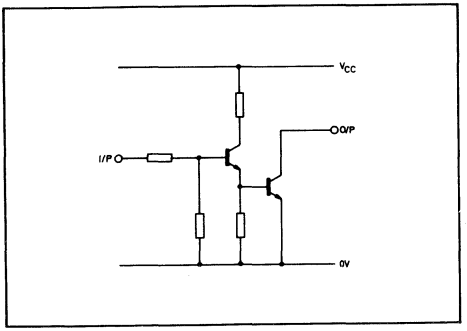


Fig. 2 Functional diagram (one driver)

ABSOLUTE MAXIMUM RATINGS

Output collector voltage	26V
Supply voltage, SP761B	+15V
Supply voltage ,SP762B	+7V
Storage temp.	−55°C to +125°C
Chip operating temp.	+125°C
Ambient operating temp.	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristic	Type	Value (note 1)			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC}	SP761B	11	12	13	V	See note 2
	SP762B	4.5	5	5.5	V	See note 2
Quiescent supply current	SP761B		8		mA	All inputs low
	SP762B		10		mA	All inputs low
On state supply current, per element	Both		12		mA	I_{IH} = 1mA
Input current I_{IH}	SP761B	1		4	mA	I_{out} = 150mA
Input voltage V_{IH}	SP761B		4		V	I_{IH} = 1mA
Input current I_{IL}	SP761B			50	μA	
Input voltage V_{IH}	SP762B	2.7		5.5	V	I_{out} = 200mA
Input current I_{IH}	SP762B		1		mA	V_{IH} = 2.7V
Input voltage V_{IL}	SP762B			1	V	
Output current I_{out}	SP761B			150	mA	I_{IH} = 1mA
	SP762B			200	mA	V_{IH} = 2.7V
Output voltage V_{OL}	SP761B		1.0	1.2	V	I_{out} = 150mA
	SP762B		1.3	1.6	V	I_{out} = 200mA
Output voltage V_{OH}	Both			26	V	
Output breakdown voltage	Both	26			V	See note 3
Duty cycle	SP761B			40	%	All outputs at I_{out} max.
	SP762B			33	%	
On time				2	s	

NOTES

1. Both 0V supply pins 1 and 7 must be connected at all times.
2. Min. and max. limits apply to the temperature range 0°C to +70°C. All typical values are quoted for V_{CC} = Typical and T_{amb} = +25°C.
3. External clamping diodes must be used when driving inductive loads.

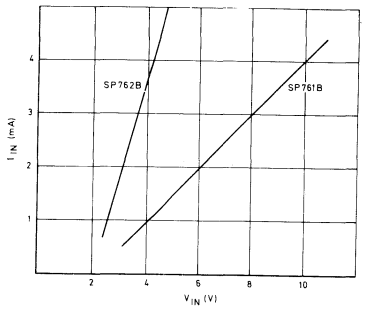


Fig. 3 Input characteristic (including strobe) T_{amb} = +25°C

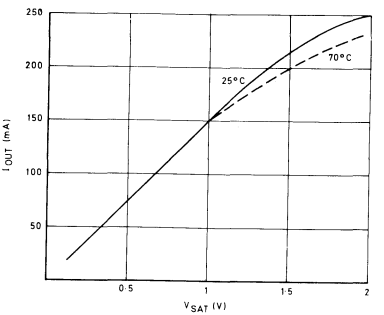


Fig. 4 Output characteristic

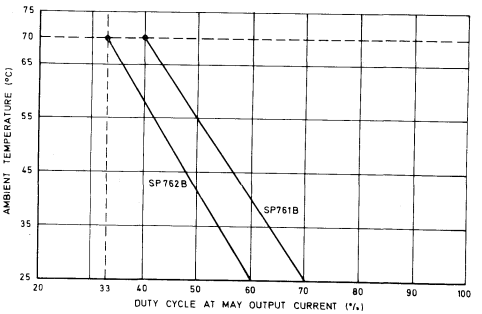


Fig. 5 Operating characteristics

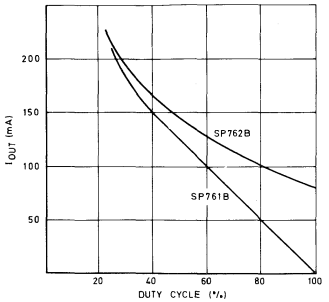


Fig. 6 Operating characteristics at +70°C

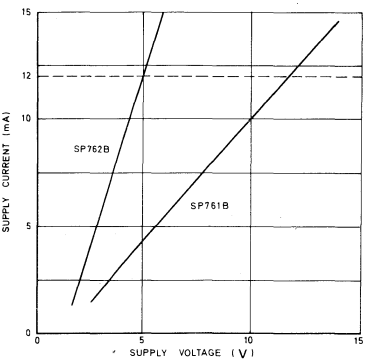


Fig. 7 On state supply current drain per element

OPERATING NOTES

Interfacing

The SP761B is designed to interface directly with MOS devices, accepting free drain input currents in the range 1 mA to 4 mA. Current limiting input resistors are incorporated on-chip to reduce power dissipation in the MOS circuit. The resistor is approximately 2 kΩ, giving an input voltage of 4V at 1 mA.

Fig. 8 shows (i) a direct interface to MOS and (ii) an interface using an external resistor to further limit input current when driven from a high voltage source.

The SP762B will interface directly with standard TTL over the temperature range 0°C to +70°C, a TTL logic '1' making current available at the SP762B output. Although TTL is not specified to source more than 400 μA at logic '1' level, the majority of gates will in fact supply approximately 5 mA and still maintain a logic '1' level in excess of 2.7V. Since the input resistors of the SP762B are approximately 600Ω, then one TTL output is capable of driving up to 5 SP762B inputs. When driving only one input of an SP762B, the input current will limit at approximately 2 mA at 3.4V. Open-collector TTL gates can also be used to drive the SP762B, provided that each TTL output has an external load resistor, the value of which will depend on the fanout required.

The characteristics of the strobe input are the same as for the individual inputs and therefore the above comments also apply to this input.

Unused Inputs

When using the strobe input, inputs 1 and 2 must be left floating. However, inputs 1 and 2 can be used completely independently in the same way as the other inputs. Any other unused inputs can either be left floating or tied to the negative supply rail.

Output Capability

The output capability of each channel is 150 mA for the SP761B and 200 mA for the SP762B. With all five drivers operating at these current levels, a duty cycle of 40% for the SP761B and 33% for the SP762B will allow operation over the temperature range 0°C to +70°C.

If the device is to be operated at a lower ambient temperature, or at a lower output current, then the duty cycle may be increased as shown in Fig. 6 and 7. Likewise, if some of the outputs are unused the duty cycle of the remaining outputs may be proportionally increased provided that the drivers are used symmetrically within the package.

The package has a thermal time constant such that the chip temperature will rise above the permitted maximum of +125°C if all the drivers are allowed to remain on at maximum output current for more than 2 seconds.

The drivers will operate at up to 1 MHz but at such frequencies the input mark/space ratio will have to be modified because the effective output duty cycle is higher than that at the inputs due to stored charge in the output transistors.

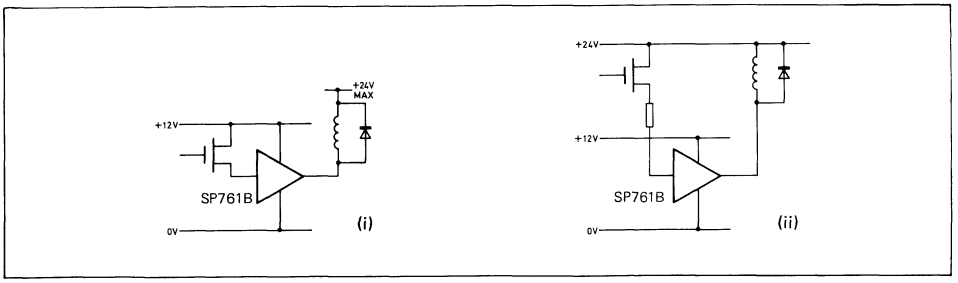


Fig. 8 Interfacing to MOS

PLESSEY
SEMICONDUCTORS

SP700 SERIES
INTERFACE CIRCUITS

NEW PRODUCT DATA

SP763 B SP764 B SP765 B

POWER INTERFACE CIRCUITS

The SP763/4/5 are bipolar integrated circuits each incorporating 10 current amplifiers for interfacing between MOS/TTL devices and loads requiring high drive currents. The SP763 and SP764 are designed to operate from an MOS compatible supply of typically +12V whereas the SP765 is designed for a TTL supply rail of +5V.

The SP764/5 are provided with a strobe input which drives two of the amplifiers so that their outputs can be connected in parallel for higher output current capability.

The circuits operate over a temperature range of 0°C to +70°C and are available in 24-lead DIL ceramic package or 24-lead DIL plastic stud (SP764B and SP765B only), for applications requiring higher dissipation.

Although primarily designed to drive printing solenoids in calculators, these circuits can be used in a variety of applications – including driving filament lamps, L.E.D.s, relays, cores and other devices requiring high drive currents e.g., power transistors.

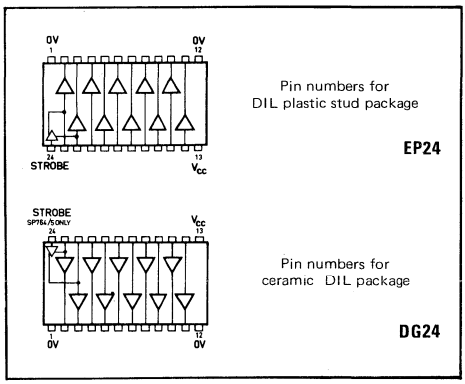


Fig. 2 Pin connections

FEATURES

- 200mA Output Capability
- MOS/TTL Compatible
- On-Chip Input Current Limiting Resistors
- Zero Standby Power
- Direct interface to Seiko and similar printers

APPLICATIONS

- Driving Solenoids
- Driving Relays
- Driving L.E.D.s
- Driving Filament Lamps
- Driving Cores
- TTL-to-MOS Translator

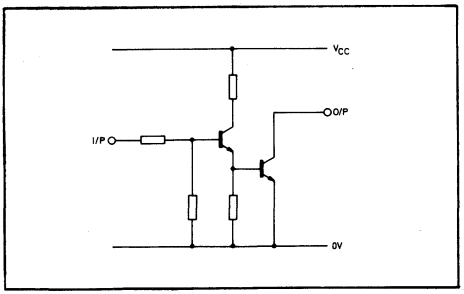


Fig. 1 One driver element

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	
SP763B & SP764B	+15V
SP765B	+7V
Storage temperature	−55°C to +125°C
Chip operating temperature	+125°C
Ambient operating temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristic	Type	Value (note 1)			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage, V_{CC}	SP763B					
	SP764B	11.0	12.0	13.0	V	Note 2
Operating supply voltage, V_{CC}	SP765B	4.5	5.0	5.5	V	
Supply current per element	SP764/765B		12.0		mA	I_{in} = 1mA
Supply current per element	SP763B		5		mA	I_{in} = 1mA
Input current, I_{IH}	SP763/764B	1		4	mA	
Input voltage, V_{IH}	SP763/764B		4		V	I_{in} = 1mA
Input current, I_{IL}	SP763/764B			50	μA	
Input voltage, V_{IH}	SP765B	2.7		5.5	V	
Input current, I_{IH}	SP765B		1		mA	V_{in} = 2.7V
Input voltage, V_{IL}	SP765B			1	V	
Strobe high input current, I_{SH}	SP764/765B	1		4	mA	
Strobe high input voltage, V_{SH}	SP764/765B		4		V	I_{SH} = 1mA
Output current, I_{out}	SP763B			50	mA	I_{in} = 1mA
Output current, I_{out}	SP764B			150	mA	I_{in} = 1mA
Output current, I_{out}	SP765B			200	mA	I_{in} = 1mA
Output voltage low, V_{OL}	SP764B		1.0	1.2	V	I_{out} = 150mA
(saturation voltage)	SP765B		1.3	1.6	V	I_{out} = 200mA
Output breakdown	SP763B	12			V	Note 3
voltage, B_{VO}	SP764/765B	26			V	Note 3
Duty cycle Ceramic package	SP763B			100	%	I_{out} = Max.
Ceramic package	SP764B			25	%	At I_{out} = Max.
Ceramic package	SP765B			25	%	I_{in} = 1mA
Plastic package	SP764B			40	%	T_A = +70°C
Plastic package	SP765B			40	%	V_{CO} = Typ.
ON time	SP764/765B			2	sec.	

NOTES

1. Min. and Max. limits apply to the guaranteed temperature range of 0°C to +70°C unless otherwise specified. All typical values are quoted for V_{CC} = Typ. and T_A = +25°C.
2. Both 0V supply pins 1 and 12 must be connected at all times.
3. External clamping diodes must be used when driving inductive loads.

Typical Performance Characteristics

In the following characteristics (Figs. 3 to 10), V_{CC} = + 12V (SP763, SP764B) or + 5V (SP765B).

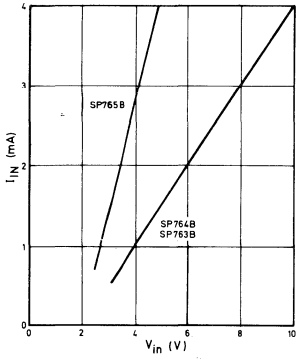


Fig. 3 Input characteristics (T_A = +25°C)

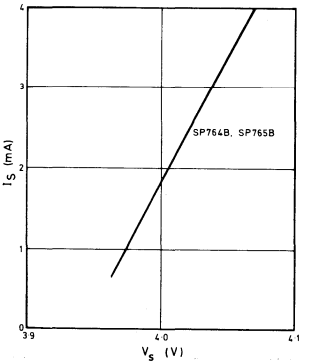


Fig. 4 Strobe input characteristics (T_A = +25°C)

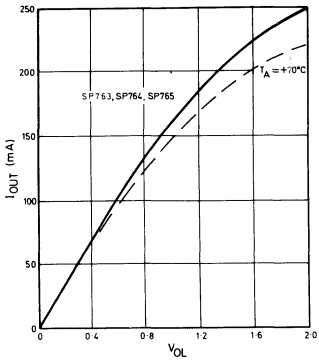


Fig. 5 Output characteristics (T_A = +25°C)

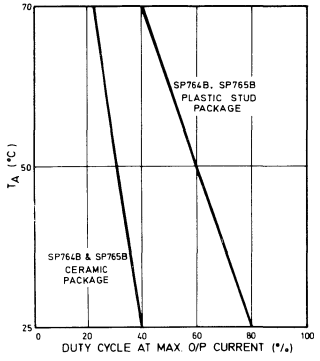


Fig. 6 Operating characteristics (T_A = +25°C to +70°C)

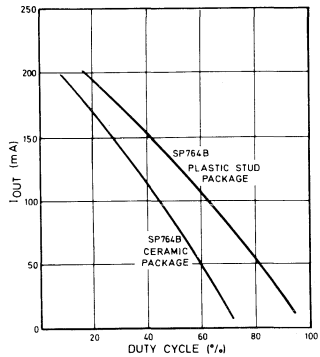


Fig. 7 SP764 operating characteristics (T_A = +70°C max.)

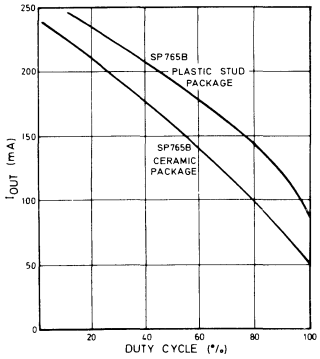


Fig. 8 SP765 operating characteristics (T_A = +70°C max.)

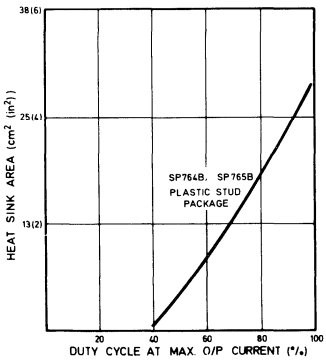


Fig. 9 Operating characteristics, stud package with heatsink (T_A = +70°C max.)

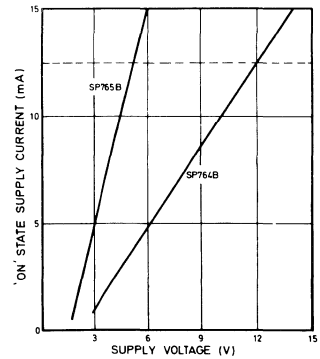


Fig. 10 Current drain per element (T_A = +70°C max.)

OPERATING NOTES

Interfacing

The SP763/764 are designed to interface directly with MOS devices, accepting free drain input currents in the range 1mA to 4mA. Current-limiting input resistors are incorporated on-chip to reduce power dissipation in the MOS circuit. The resistor is approximately 2kΩ giving an input voltage of 4V at 1mA (see Figs.3 and 4).

Fig.11 shows (i) a direct interface to MOS and (ii) an interface using an external resistor to further limit input current when driven from a high voltage source.

The SP765B will interface directly with standard TTL over the temperature range 0°C to +70°C, a TTL logic '1' making current available at the SP765 driver output. Although TTL is not specified to source more than 400μA at the logic '1' level, a typical gate will in fact supply approximately 5mA and still maintain a logic '1' level of about +2.7V. Since the input current – limiting resistors on the SP765 are approximately 700Ω (giving an input voltage of +2.7V at 1mA) then one TTL output is capable of driving up to 5 SP765 inputs. If, however, a TTL gate is used to drive only one SP765 input, then the current will limit at approximately 2mA, corresponding to an input voltage of +3.4V. Open-collector TTL gates can also be used to drive SP765s but in such cases each TTL output must have an external load resistor, the value of which will depend on the fanout required.

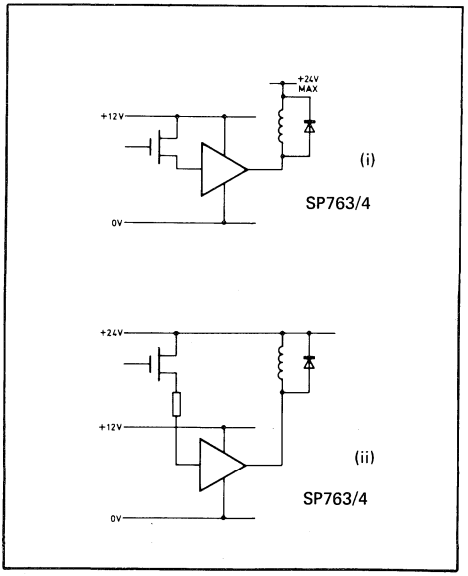


Fig. 11 Interfacing SP763/SP764 to MOS

Strobe Input

A positive voltage (as defined in the Electrical Characteristics) applied to the strobe input (pin 24) enables drivers 1 and 2 simultaneously. Thus, using this input permits output current sinking of up to 300 mA (SP764B) and 400 mA (SP765B) by connecting together outputs 1 and 2 (pins 2 and 3).

No current limiting resistor is provided at the strobe input as the input voltage at 1mA is 4V on all circuit variants (see Fig.4). When using the SP765B, therefore, the strobe input must be driven either from an open-collector TTL gate with an appropriate load resistor or from a normal TTL gate with an external 1kΩ resistor between its output and V_{CC} as shown in Fig.12.

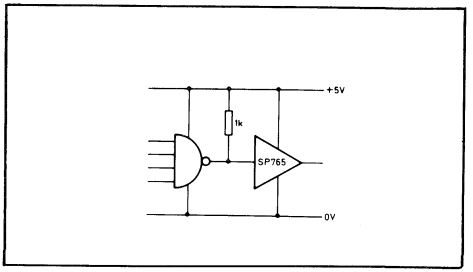


Fig.12 TTL interface to SP765 strobe input

Unused Inputs

When using the strobe input, inputs 1 and 2 must be left floating. However, inputs 1 and 2 can be used completely independently, in the same way as the other inputs. Any other unused inputs can either be left floating or tied to the negative supply rail.

Output Capability

The SP763B has an output rating for each driver of 50mA and may be used over the full temperature range of 0°C to +70°C at 100% duty cycle.

The SP764B has an output rating of 150mA for each driver and the SP765B a rating of 200mA. With all ten drivers operating at these current levels a duty cycle of 25% for the ceramic package and 40% for the plastic stud package will allow operation over the temperature range 0°C to +70°C.

If a lower ambient operating temperature can be tolerated, then the duty cycle may be increased up to a maximum of 40% (ceramic) and 80% (plastic stud) at +25°C. Operation of the drivers at lower output currents will also allow the duty cycle to be increased, as shown in Figs.6, 7, 8 and 9. In addition, if some of the outputs are unused, then the duty cycle of the remaining outputs may be increased, provided that the drivers are used symmetrically within the package. For example, if outputs 5 and 6 are not used, then the duty cycle of the remaining 8 outputs can be increased in the ratio 10:8.

The drivers will operate at up to 1MHz but at such frequencies the input signal mark/space ratio will have to be modified because the effective output duty cycle is higher than that of the inputs due to charge storage in the output transistors.

Because of the high current levels which the drivers are capable of making it is essential that both the O_V pins should be connected. The track resistance to each pin should be approximately equal to ensure equal current sharing.

Plastic Stud Package

With the addition of a heat risk of thermal resistance not greater than 12°C/Watt, operation at up to 100% duty cycle (i.e. D.C. operation at maximum output current) can be achieved over the full temperature range 0°C to +70°C. A suitable heat sink consists of 25 cm^2 (4 in^2) of 16 SWG Aluminium folded as shown in Fig. 13.

Note: On the stud package, the stud is connected to the negative rail.

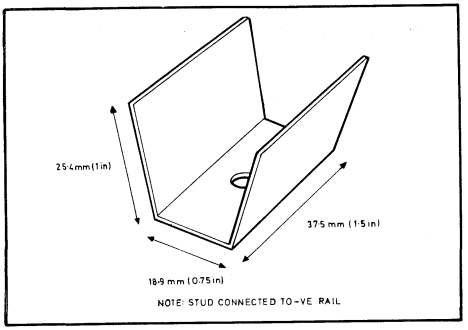


Fig. 13 Heatsink details for stud package

Typical Application

A typical calculator application for SP764/SP765 devices is shown in Fig. 14. In this, two packages are required to drive the 18 printing solenoids and the paper/ribbon feed solenoid. The 10 drivers in one package are used to drive 10 printing solenoids and the remaining 8 solenoids are driven by outputs 3 to 10 of the second package. The paper/ribbon feed solenoid is controlled by the strobe input of the second package and driven by the parallel outputs 1 and 2.

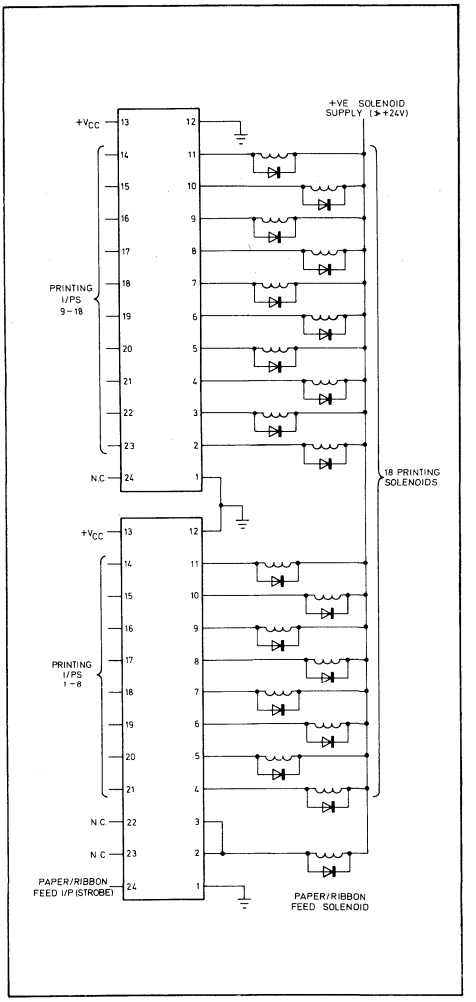


Fig. 14 Typical printing calculator application

PLESSEY
SEMICONDUCTORS

SP1404

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

CIRCUIT DESCRIPTION (FIG. 2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs an inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to ($V_{CC}-1$) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

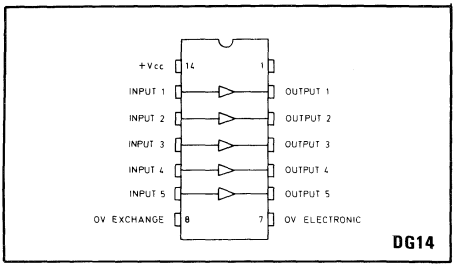


Fig. 1 Pin connections (viewed from underside)

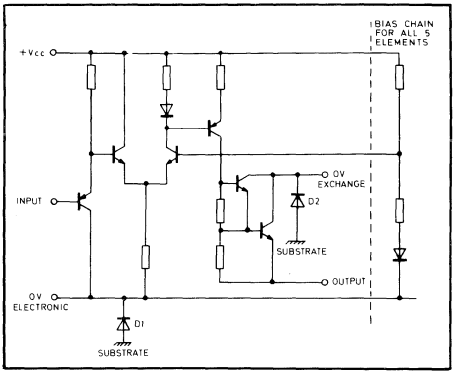


Fig. 2 Circuit diagram of one element

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
Temperature range = 0°C to +70°C
V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		−20		μA	V_{in} = 0V
		−2		μA	V_{in} = V_{cc}
Output voltage			1.5	V	V_{in} = 0.8V, I_{out} = 50mA
Output current			100	μA	V_{in} = 2V, V_{out} = 60V
V_{CC} supply current		30		mA	V_{cc} = 5V, all inputs low
Total power dissipation		450		mW	V_{cc} = 5V, all inputs low all outputs I_{out} = 50mA

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{out} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy' earth	−65V
V_{cc} to output voltage	75V
V_{cc} to electronic earth	7V
Input voltage	V_{cc} + 1V

PLESSEY
SEMICONDUCTORS

SP10,000 SERIES

ECL 10,000

ECL 10,000 has an excellent speed-power product, has relatively low rise and fall times, and transmission-line capability. The combination of varsatile logic functions and the 2.0ns propagation delay make ECL 10,000 a versatile family for data handling and processing systems.

Circuit design with ECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. ECL III is directly compatible with ECL 10,000 and can be used to extend the speed capability of the ECL 10,000 series.

The SP 10,000 series are a direct second source for the Motorola MC 10,000 and MCM 10,000 series.

FUNCTIONS AND CHARACTERISTICS @ V_{CC}=0, V_{EE}=–5.2V, T_A=+25°C

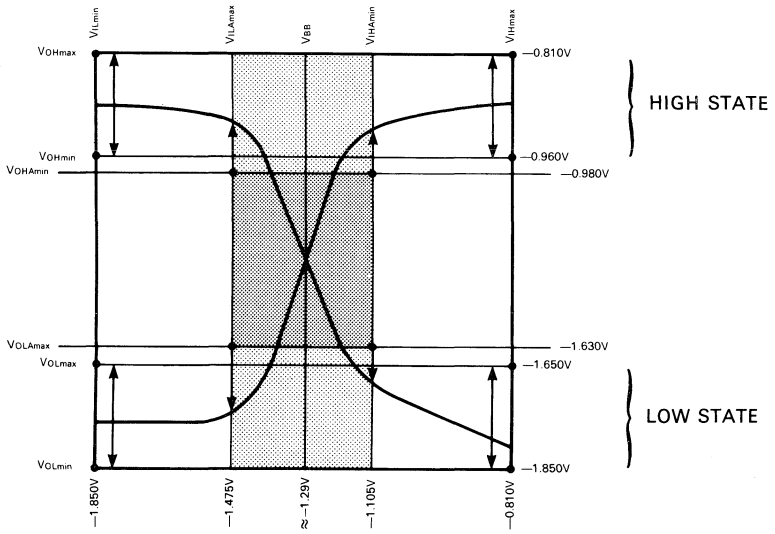
Function	Type	Propagation Delay ns typ.	Power Dissipation* mW typ/pkg
Quad 2-I/P NOR gate with strobe	SP10100	2.0	100
Quad OR/NOR gate	SP10101	2.0	100
Quad 2-I/P NOR gate	SP10102	2.0	100
Quad 2-I/P OR gate	SP10103	2.0	100
Quad 2-I/P AND gate	SP10104	2.7	140
Triple 2-3-2-I/P OR/NOR gate	SP10105	2.0	90
Triple 4-3-3-I/P NOR gate	SP10106	2.0	90
Triple 2-I/P exclusive OR/exclusive NOR	SP10107	2.5	110
Dual 4-5-I/P OR/NOR gate	SP10109	2.0	60
Dual 3-I/P 3-O/P OR gate	SP10110	2.4	160
Dual 3-I/P 3-O/P NOR gate	SP10111	2.4	160
Dual 3-I/P 3-O/P OR/NOR gate	SP10112	2.4	160
Quad exclusive OR gate	SP10113	2.5	175
Triple line receiver	SP10114	2.4	145
Quad line receiver	SP10115	2.0	110
Triple line receiver	SP10116	2.0	85
Dual 2-wide 2-3-I/P OR-AND/OR-AND Invert gate	SP10117	2.3	100
Dual 2-wide 3-I/P OR/AND gate	SP10118	2.3	100
4-wide 4-3-3-3-I/P OR/AND gate	SP10119	2.3	100
4-wide OR-AND/OR-AND Invert gate	SP10121	2.3	100
Quad TTL to ECL translator	SP10124	3.5	380
Quad ECL to TTL translator	SP10125	4.5	380
Bus driver	SP10128	12	700
Quad bus receiver	SP10129	10.0	750
Dual latch	SP10130	2.5	155
Dual type D master slave flip-flop	SP10131	f=160MHz	235
Multiplexer with latch	SP10134	3.0	225
Dual J-K master-slave flip-flop	SP10135	f=140MHz	280
Universal hexadecimal counter	SP10136	f=150MHz	625
Universal decade counter	SP10137	f=150MHz	625
Bi-quinary counter	SP10138	f=150MHz	370
64-bit random access memory	SP10140	t_{access}=15ns (max)	420
Four-bit universal shift register	SP10141	f=200MHz	425
64-bit random access memory	SP10142	t_{access}=10ns (max)	420
256-bit random access memory	SP10144	t_{access}=30ns (max)	420
64-bit register file (RAM)	SP10145	t_{access}=10ns (typ)	625
1024-bit random access memory	SP10146		
64-bit random access memory	SP10148	t_{access}=15ns (max)	420
12-bit parity generator checker	SP10160	5.0	320
Binary to 1 out of 8 decoder (low)	SP10161	4.0	315
Binary to 1 out of 8 decoder (high)	SP10162	4.0	315
8-line multiplexer	SP10164	3.0	310
8-input priority encoder	SP10165	7.0	545
Dual binary to 1 out of 4 decoder (low)	SP10171	4.0	325
Dual binary to 1 out of 4 decoder (high)	SP10172	4.0	325
Quad 2-I/P multiplexer/latch	SP10173	2.5	275
Dual 4 to 1 multiplexer	SP10174	3.5	305
Quint latch	SP10175	2.5	400
Hex D master-slave flip-flop	SP10176	f=250MHz	460
Binary counter	SP10178	f=150MHz	370
Look-ahead carry block	SP10179	3.0 (Cn,P) 4.0 (G)	300
Dual high speed adder/subtractor	SP10180	4.5	360
4-bit arithmetic logic unit/function generator	SP10181	See logic diag.	600

* Load power not included

TYPICAL TRANSFER CHARACTERISTICS OF ECL10100 FAMILY

Test conditions: T_A = +25 °C, V_{EE} = −5.2V, 50Ω matched inputs and outputs.

PARAMETER	−30 °C	+25 °C	+85 °C
V_{IHmax}	−0.890V	−0.810V	−0.700V
V_{ILmin}	−1.890V	−1.850V	−1.825V
V_{IHAmin}	−1.205V	−1.105V	−1.035V
V_{ILAmax}	−1.500V	−1.475V	−1.440V
V_{OHmax}	−0.890V	−0.810V	−0.700V
V_{OLmin}	−1.890V	−1.850V	−1.825V
V_{OHmin}	−1.060V	−0.960V	−0.890V
V_{OLmax}	−1.675V	−1.650V	−1.615V
V_{OHAmin}	−1.080V	−0.980V	−0.910V
V_{OLAmax}	−1.655V	−1.630V	−1.595V



ABSOLUTE MAXIMUM RATINGS

A. Limits beyond which device life may be impaired:

Power supply voltage, V_{EE} (V_{CC} = 0)		−8V to 0V
Base input voltage, V_{in} (V_{CC} = 0)		0V to V_{EE}
Output source current, I_O :-		
	Continuous	<50mA
	Surge	<100mA
Storage temperature, T_{stg}		−55 °C to 150 °C
*Junction operating temperature, T_j :-		
	Plastic package	<150 °C
	Ceramic package	<165 °C

B. Limits beyond which performance may be degraded:

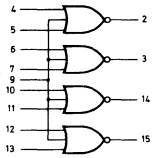
Operating temperature range, T_A	−30 °C to +85 °C
DC fan-out	<70
Power supply regulation	±10%

*T_{case} must be<150 °C

LOGIC DIAGRAMS

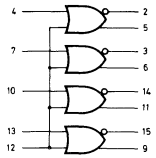
Positive logic is used throughout.
Power supply connections:
V_{CC1}=pin 1, V_{CC2}=pin 16, V_{EE}=pin 8,
except where otherwise stated.

SP10100
QUAD 2-INPUT NOR GATE WITH STROBE



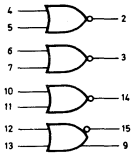
P_D=25mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10101
QUAD OR/NOR GATE



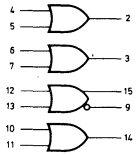
P_D=25mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10102
QUAD 2-INPUT NOR GATE



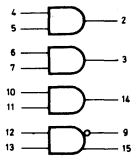
P_D=25mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10103
QUAD 2-INPUT OR GATE



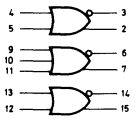
P_D=25mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10104
QUAD 2-INPUT AND GATE



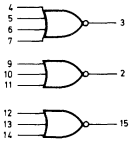
P_D=35mW typ/gate (No load)
t_{pd}=2.7ns typ

SP10105
TRIPLE 2-3-2 INPUT OR/NOR GATE



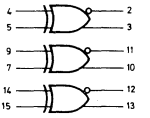
P_D=30mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10106
TRIPLE 4-3-3 INPUT NOR GATE



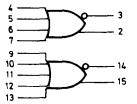
P_D=30mW typ/gate (No load)
t_{pd}=2.0ns typ

SP10107
TRIPLE 2-INPUT EXCLUSIVE OR/EXCLUSIVE NOR



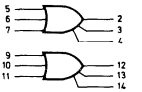
P_D=110mW typ/pkg (No load)
t_{pd}=2.5ns typ

SP10109
DUAL 4-5-INPUT OR/NOR GATE



P_D=30mW typ/gate (No load)
t_{pd}=2.0ns typ

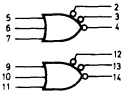
SP10110
DUAL 3-INPUT 3-OUTPUT OR GATE



V_{CC1} = pins 1 and 15
V_{CC2} = pin 16
V_{EE} = pin 8

P_D=160mW typ/pkg (No load)
t_{pd}=2.4ns typ

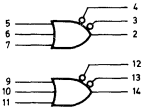
SP10111
DUAL 3-INPUT 3-OUTPUT NOR GATE



V_{CC1} = pins 1 and 15
V_{CC2} = pin 16
V_{EE} = pin 8

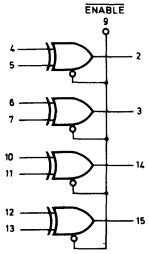
P_D=160mW typ/pkg (No load)
t_{pd}=2.4ns typ

SP10112
DUAL 3-INPUT 3 OUTPUT OR/NOR GATE



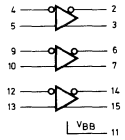
P_D=160mW typ/pkg (No load)
t_{pd}=2.4ns typ

SP10113
QUAD EXCLUSIVE OR GATE
TO BE ANNOUNCED



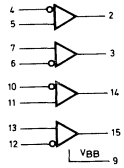
P_D=175m typ/pkg (No load)
t_{pd}=2.5ns typ

SP10114
TRIPLE LINE RECEIVER
TO BE ANNOUNCED



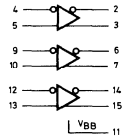
t_{pd}=2.4ns typ (Single ended input)
t_{pd}=2.0ns (Differential input)
P_D=145mW typ/pkg (No load)

SP10115
QUAD LINE RECEIVER



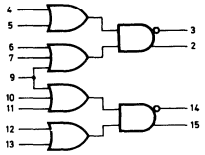
P_D=110mW typ/pkg (No load)
t_{pd}=2.0ns typ

SP10116
TRIPLE LINE RECEIVER
TO BE ANNOUNCED



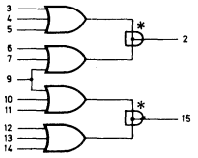
P_D=85mW typ/pkg (No load)
t_{pd}=2.0ns typ

SP10117
DUAL 2-WIDE 2-3-INPUT OR-AND/OR-AND-INVERT GATE



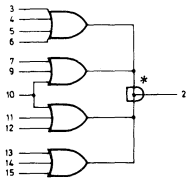
P_D=100mW typ/pkg (No load)
t_{pd}=2.3ns typ

SP10118
DUAL 2-WIDE 3-INPUT OR-AND GATE



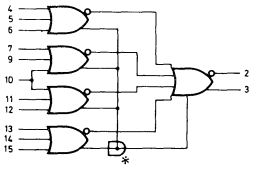
*Collector dot
P_D=100mW typ/pkg (No load)
t_{pd}=2.3ns typ

SP10119
4-WIDE 4-3-3-3 INPUT OR-AND GATE



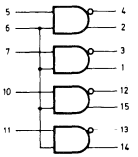
*Collector dot
P_D=100mW typ/pkg (No load)
t_{pd}=2.3ns typ

SP10121
4-WIDE OR-AND/OR-AND INVERT GATE



*Collector dot
P_D=100 mW typ/pkg (No load)
t_{pd}=2.3ns typ

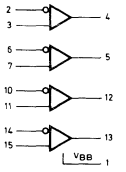
SP10124
QUAD TTL TO ECL TRANSLATOR



V_{CC} (+5V)=pin 9
V_{EE} (−5.2V)=pin 8
Gnd=pin 16

P_D=380mW typ/pkg (No load)
t_{pd}=3.5ns typ (50% to +1.5 Vdc out)

SP10125
QUAD ECL TO TTL TRANSLATOR



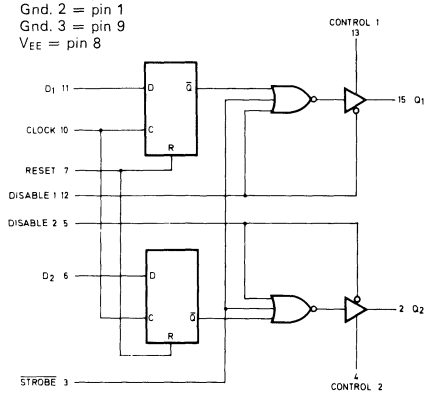
V_{CC} (+5V)=pin 9
V_{EE} (−5.2V)=pin 8
Gnd=pin 16

P_D=380mW typ/pkg (No load)
t_{pd}=3.5ns typ (50% to +1.5 Vdc out)

SP10128
BUS DRIVER

V_{CC} = pin 14
Gnd. 1 = pin 16
Gnd. 2 = pin 1
Gnd. 3 = pin 9
V_{EE} = pin 8

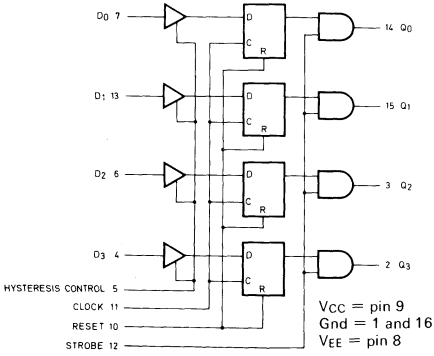
TO BE ANNOUNCED



P_D = 700 mW/pkg typ (no load)
t_{pd} = 12ns typ

SP10129
QUAD BUS RECEIVER

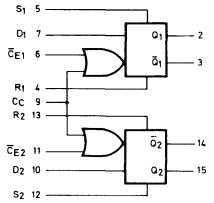
TO BE ANNOUNCED



V_{CC} = pin 9
Gnd = 1 and 16
V_{EE} = pin 8

P_D=750mW type/pkg (No load)
t_{pd}=10ns typ

SP10130
DUAL LATCH



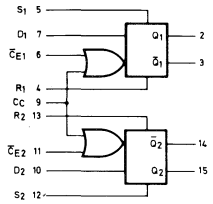
P_D=155mW typ/pkg
t_{pd}=2.5ns typ

TRUTH TABLE

D	$\overline{C}$	$\overline{C}E$	Q_n+1
L	L	L	L
H	L	L	H
ø	L	H	Q_n
ø	H	L	Q_n
ø	H	H	Q_n

ø=Don't Care

SP10131
DUAL TYPE D MASTER SLAVE FLIP-FLOP



P_D=235mW typ/pkg (No load)
f=160MHz typ

CLOCKED TRUTH TABLE

C	D	Q_n-1
L	ø	Q_n
H	L	L
H	H	H

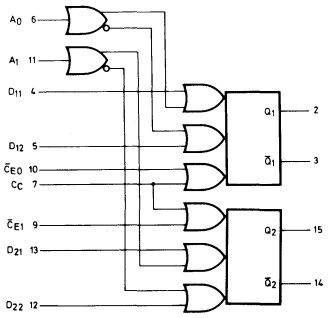
ø=Don't Care
$C=\overline{C}_E+C_C$.
A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_n-1
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

SP10134
DUAL MULTIPLEXER WITH LATCH

TO BE ANNOUNCED



P_D=225mW typ/pkg (No load)
t_{pd}=3.0ns typ

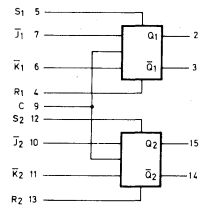
TRUTH TABLE

C	A0	D11	D12	Q_n+1
L	L	L	ø	L
L	L	H	ø	H
L	H	ø	L	L
L	H	ø	H	H
H	ø	ø	ø	Q_n

ø=Don't Care
$C=\overline{CE}+C_C$

SP10135
DUAL J-K MASTER-SLAVE FLIP-FLOP

TO BE ANNOUNCED



P_D=280mW typ/pkg (No load)
f_{tog}=140MHz typ

R-S TRUTH TABLE

R	S	Q_n+1
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

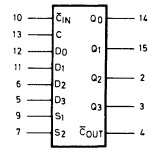
N.D.=Not Defined

CLOCK J-K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_n+1
L	L	Q_n
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

SP10136
UNIVERSAL HEXADECIMAL COUNTER



P_D=425mW typ/pkg
f_{shift}=200MHz typ

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE*

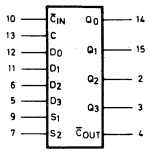
INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry}}$ In	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry}}$ Out
L	L	L	L	H	H	ø	H	L	L	H	H	L
L	H	ø	ø	ø	ø	L	H	H	L	H	H	H
L	H	ø	ø	ø	ø	L	H	L	H	H	H	H
L	H	ø	ø	ø	ø	L	H	H	H	H	H	L
L	H	ø	ø	ø	ø	H	L	H	H	H	H	H
L	H	ø	ø	ø	ø	H	H	H	H	H	H	H
H	H	ø	ø	ø	ø	ø	H	H	H	H	H	H
L	L	H	H	L	L	ø	H	H	H	L	L	L
H	L	ø	ø	ø	ø	L	H	L	H	L	L	H
H	L	ø	ø	ø	ø	L	H	H	L	L	L	H
H	L	ø	ø	ø	ø	L	H	L	L	L	L	L
H	L	ø	ø	ø	ø	L	H	H	H	H	H	H

ø=Don't care.

*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

**A clock H is defined as a clock input transition from a low to a high logic level.

SP10137
UNIVERSAL DECADE COUNTER



P_D=625mW typ/pkg (No load)
f_{count}=150MHz typ

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

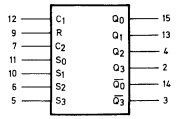
SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry}}$ In	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry}}$ Out
L	L	H	H	H	L	ø	H	H	H	H	L	H
L	H	ø	ø	ø	ø	L	H	L	L	L	H	H
L	H	ø	ø	ø	ø	L	H	H	L	L	H	L
L	H	ø	ø	ø	ø	L	H	L	L	L	L	H
L	H	ø	ø	ø	ø	L	H	H	L	L	L	H
L	H	ø	ø	ø	ø	H	H	H	L	L	L	H
L	H	ø	ø	ø	ø	H	H	H	L	L	L	H
H	H	ø	ø	ø	ø	ø	H	H	L	L	L	H
L	L	H	H	L	L	ø	H	H	H	L	L	H
H	L	ø	ø	ø	ø	L	H	L	H	L	L	H
H	L	ø	ø	ø	ø	L	H	H	L	L	L	H
H	L	ø	ø	ø	ø	L	H	L	L	L	L	L

ø = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
**A clock H is defined as a clock input transition from a low to a high logic level.

SP10138
BI-QUINARY COUNTER

TO BE ANNOUNCED



P_D = 370 mW typ/pkg (no load)
f_{tog} = 150 MHz typ

COUNTER TRUTH TABLES

BI-QUINARY

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

(Clock connected to C2 and $\overline{Q3}$ connected to C1)

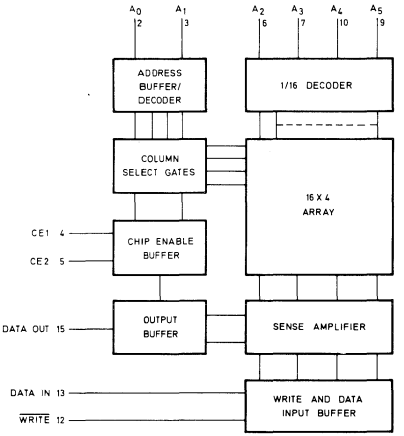
BCD

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(Clock connected to C1 and $\overline{Q0}$ connected to C2)

SP10140 (90Ω)
SP10142 (50Ω)
SP10148 (50Ω)
64-BIT RANDOM MEMORY

TO BE ANNOUNCED



P_D = 420 mW typ /pkg
t_{access} = 15ns (max) SP10140, SP10148
= 10ns (max) SP10142

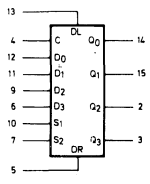
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø = Don't Care

SP10141
FOUR-BIT UNIVERSAL SHIFT REGISTER

TO BE ANNOUNCED



P_D=425mW typ/pkg
f_{shift}=200MHz typ

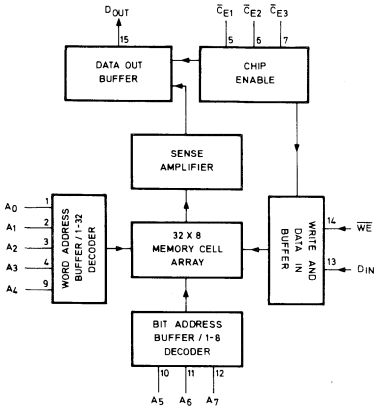
TRUTH TABLE

SELECT		OPERATING	OUTPUTS			
S1	S2	MODE	$Q0_n+1$	$Q1_n+1$	$Q2_n+1$	$Q3_n+1$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse=Positive transition of clock input).

SP10144
256-BIT RANDOM ACCESS MEMORY

TO BE ANNOUNCED



t_{access}=30ns (max) (Address inputs)

TRUTH TABLE

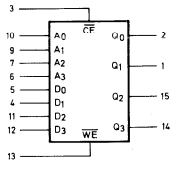
MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø=Don't Care

SP10145
64-BIT REGISTER FILE (RAM)

TO BE ANNOUNCED

V_{CC} = pin 16
V_{EE} = pin 8



P_D = 625 mW typ. pkg. (no load)
t_{access} = 10ns typ

TRUTH TABLE

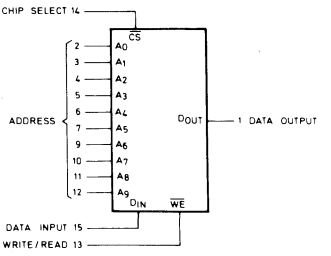
MODE	INPUT			OUTPUT
	CE	WE	D	Q
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø = Don't Care.

SP10146
1024 BIT RANDOM ACCESS MEMORY

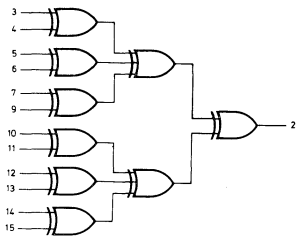
TO BE ANNOUNCED

V_{CC}=pin 16
V_{EE}=pin 8



SP10160
12-BIT PARITY GENERATOR CHECKER

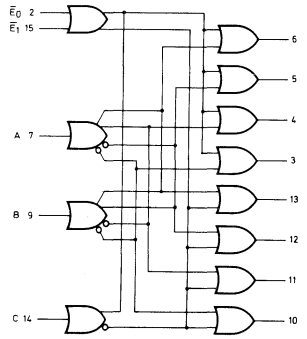
TO BE ANNOUNCED



P_D=320mW typ/pkg (No load)
t_{pd}=5.0ns typ

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

SP10161
BINARY TO 1 OUT OF 8 DECODER (LOW)



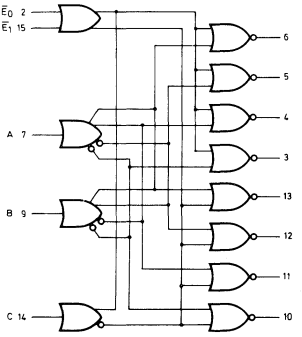
P_D=315mW typ/pkg (No load)
t_{pd}=4.0ns typ

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	ø	ø	ø	ø	H	H	H	H	H	H	H	H
ø	H	ø	ø	ø	H	H	H	H	H	H	H	H

ø=Don't Care

SP10162
BINARY TO 1 OUT OF 8 DECODER (HIGH)



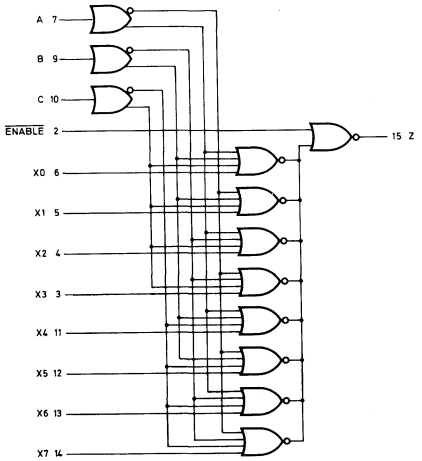
P_D=315mW typ/pkg (No load)
t_{pd}=4.0ns typ

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E0}$	$\overline{E1}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ø	ø	ø	ø	L	L	L	L	L	L	L	L
ø	H	ø	ø	ø	L	L	L	L	L	L	L	L

ø=Don't Care

SP10164
8-LINE MULTIPLEXER



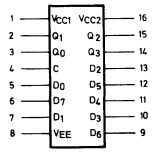
P_D=310mW typ/pkg (No load)
t_{pd}=3.0ns typ

TRUTH TABLE

	ADDRESS INPUTS			
ENABLE	C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ø	ø	ø	L

ø=Don't Care

SP10165
8-INPUT PRIORITY ENCODER
TO BE ANNOUNCED



P_D=545mW typ/pkg
t_{pd}=7.0ns typ (Data to output)

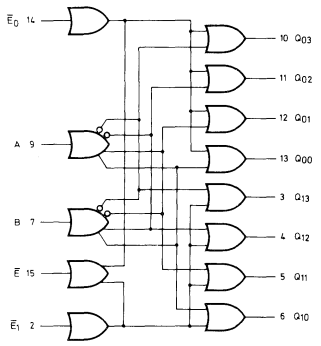
TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ø	ø	ø	ø	ø	ø	ø	H	L	L	L
L	H	ø	ø	ø	ø	ø	ø	H	L	L	H
L	L	H	ø	ø	ø	ø	ø	H	L	H	L
L	L	L	H	ø	ø	ø	ø	H	L	H	H
L	L	L	L	H	ø	ø	ø	H	H	L	L
L	L	L	L	L	H	ø	ø	H	H	L	H
L	L	L	L	L	L	H	ø	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ø=Don't Care

SP10171
DUAL BINARY TO 1 OUT OF 4 DECODER
(LOW)

P_D=325mW typ/pkg (No load)
t_{pd}=4.0ns typ



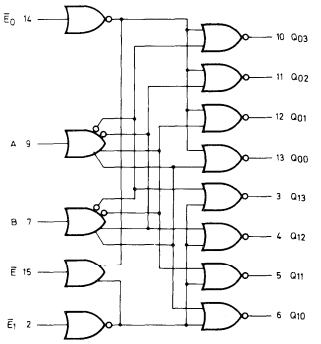
TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E0}$	$\overline{E1}$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	L	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ø	ø	ø	ø	H	H	H	H	H	H	H	H

ø=Don't Care

SP10172
DUAL BINARY TO 1 OUT OF 4 DECODER
(HIGH)

P_D=325mW typ/pkg (No load)
t_{pd}=4.0ns typ



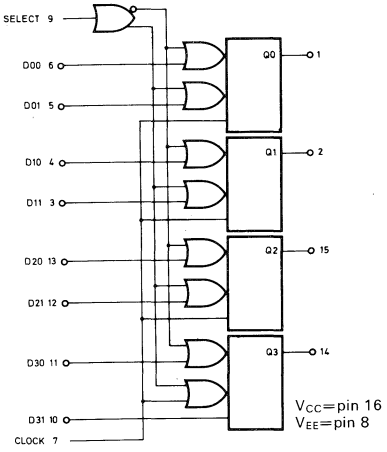
TRUTH TABLE

$\overline{E}$	$\overline{E1}$	$\overline{E0}$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	ø	ø	ø	ø	L	L	L	L	L	L	L	L

ø=Don't Care

SP10173
QUAD 2-INPUT MULTIPLEXER/LATCH

TO BE ANNOUNCED



P_D=275mW typ/pkg (No load)
t_{pd}=2.5ns typ

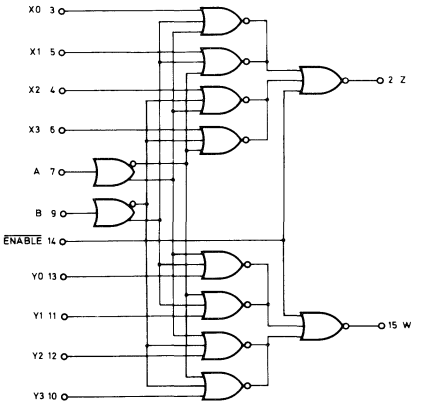
TRUTH TABLE

SELECT	CLOCK	$Q0_n+1$
H	L	D00
L	L	D01
ø	H	$Q0_n$

ø=Don't Care

SP10174
DUAL 4 TO 1 MULTIPLEXER

TO BE ANNOUNCED



P_D=155mW typ/pkg
t_{pd}=2.5ns typ

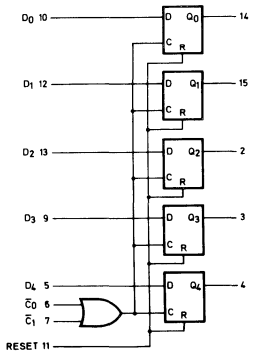
TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ø	ø	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ø=Don't Care

SP10175
QUINT LATCH

TO BE ANNOUNCED



P_D=400mW typ/pkg (No load)
t_{pd}=2.5ns typ

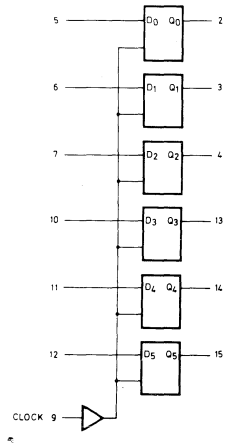
TRUTH TABLE

D	C0	C1	Reset	Q_n-1
L	L	L	L	L
H	L	L	L	H
ø	H	ø	L	Q_n
ø	ø	H	L	Q_n
ø	H	ø	H	L
ø	ø	H	H	L

ø=Don't Care

SP10176
HEX D MASTER-SLAVE FLIP-FLOP

TO BE ANNOUNCED



P_D=460mW typ/pkg (No load)
f_{tog}=150MHz

CLOCKED TRUTH TABLE

C	D	Q_n+1
L	ø	Q_n
H*	L	L
H*	H	H

ø= Don't Care
*A clock H is a clock transition from a low to a high state.

TRUTH TABLE

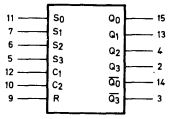
INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ø	ø	L	L	L	L
L	H	H	H	H	ø	ø	H	H	H	H
L	L	L	L	L	H	ø	No count			
L	L	L	L	L	ø	H	No count			
L	L	L	L	L		*	L	L	L	L
L	L	L	L	L		*	H	L	L	L
L	L	L	L	L		*	L	H	L	L
L	L	L	L	L		*	H	H	L	L
L	L	L	L	L		*	L	L	H	L
L	L	L	L	L		*	H	L	H	L
L	L	L	L	L		*	L	H	H	L
L	L	L	L	L		*	H	H	H	L
L	L	L	L	L		*	L	L	L	H
L	L	L	L	L		*	H	L	L	H
L	L	L	L	L		*	L	H	L	H
L	L	L	L	L		*	H	H	L	H
L	L	L	L	L		*	L	L	H	H
L	L	L	L	L		*	H	L	H	H
L	L	L	L	L		*	L	H	H	H
L	L	L	L	L		*	H	H	H	H

ø Don't Care

* Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

SP10178
BINARY COUNTER

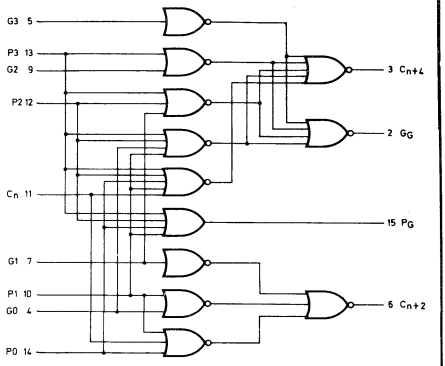
TO BE ANNOUNCED



P_D = 370 mW typ/pkg (no load)
f_{tog} = 150 MHz typ

SP10179
LOOK-AHEAD CARRY BLOCK

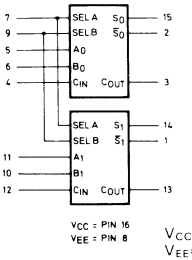
TO BE ANNOUNCED



P_D=300mW typ/pkg
t_{pd}=3.0ns typ (Carry, Propagate)
4.0ns typ (Generate)

SP10180
DUAL HIGH SPEED ADDER/SUBTRACTOR

TO BE ANNOUNCED



V_{CC}=pin 16
V_{EE}=pin 8

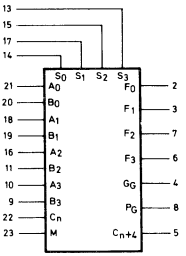
FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S=A plus B
H	L	S=A minus B
L	H	S=B minus A
L	L	S=0 minus A minus B

P_D=360mW typ/pkg
t_{pd} (typ):
C_{in} to C_{out}=2.2ns
A0 to S0=4.5ns
A0 to C_{out}=4.5ns

SP10181
4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

TO BE ANNOUNCED



V_{CC1}=pin 1
V_{CC2}=pin 24
V_{EE}=pin 12

P_D=600mW typ/pkg (No load)
t_{pd} (typ): A1 to F=6.5ns
C_n to C_{n-4}=3.1ns
A1 to P_G=0.5ns
A1 to G_G=4.5ns
A1 to C_{n-4}=5.0ns

IMPORTANT!

ECLIII Temperature Range

Since the SP1600 series datasheets were prepared, the operating temperature range of all these ECLIII products has been uprated to −30°C to +85°C, and not 0°C to +75°C as stated in the individual datasheets.

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

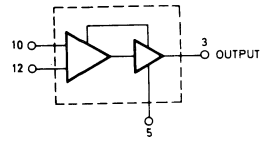
SP1648B
VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with PECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8



Input Capacitance = 6pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ.
Power Dissipation = 150mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 Mhz typ

DG14

Fig. 1 Block diagram of SP1648

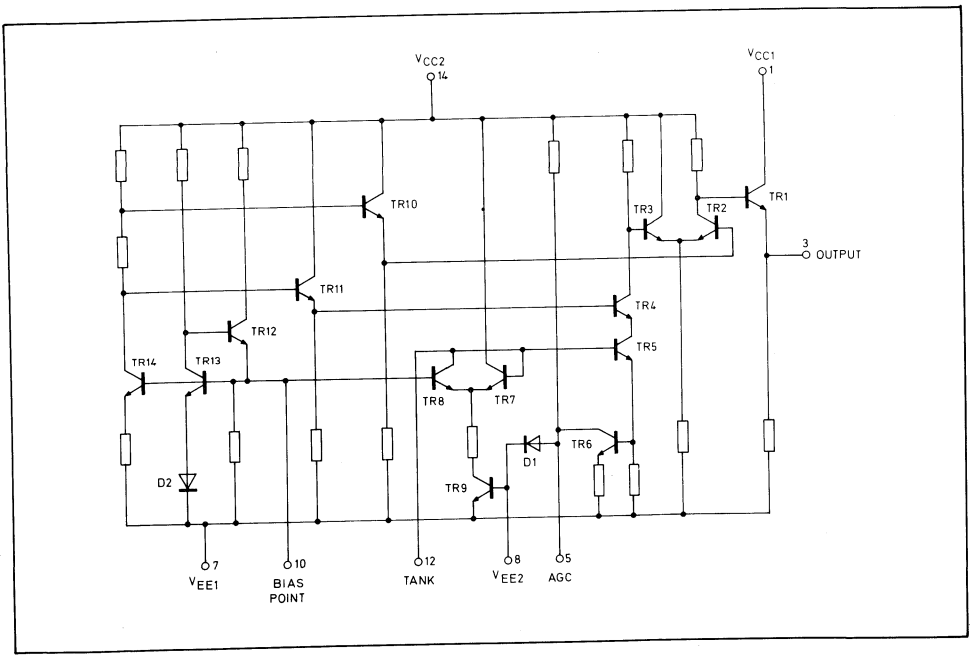


Fig. 2 Circuit diagram of SP1648

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
0°C	+1.900	+1.400	5.0	−5.0
+25°C	+1.800	+1.300	5.0	−5.0
+75°C	+1.700	+1.200	5.0	−5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	35	–	–	mAdc	–	–	1, 14		7, 8
Logic "1" Output Voltage	V_{OH}	3	4.00	4.16	4.04	4.19	4.10	4.28	Vdc	–	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.18	3.42	3.20	3.43	3.22	3.46	Vdc	12	–	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.45	1.8	1.4	1.7	1.3	1.6	Vdc	–	–	1, 14	–	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	$V_{p\text{-}p}$	12	–	– –	–	500 –	–	– –	mV	See Figure 4	–	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	–	– –	–	50 –	–	– –	%	See Figure 4	–	1, 14	3	7, 8
Oscillation Frequency	f_{max}	–	–	– –	195	225 –	–	– –	MHz	See Figure 4	–	1, 14	3	7, 8

* This measurement guarantees the dc potential at the bias for purposes of incorporating a varactor diode at this point

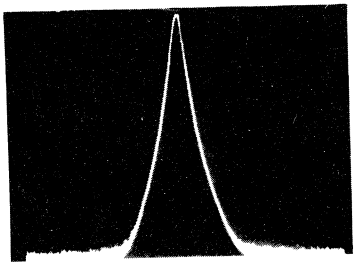
ELECTRICAL CHARACTERISTICS

Supply Voltage = −5.2 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
0°C	−3.300	−3.800	−5.2	−5.0
+25°C	−3.400	−3.900	−5.2	−5.0
+75°C	−3.500	−4.000	−5.2	−5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	36	–	–	mAdc	–	–	7, 8	–	1, 14
Logic "1" Output Voltage	V_{OH}	3	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	12	–	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	−3.750	−3.400	−3.800	−3.500	−3.900	−3.600	Vdc	–	–	7, 8	–	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Voltage	$V_{p\text{-}p}$	12	–	– –	–	500 –	–	– –	mV	See Figure 4	–	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	–	– –	–	50 –	–	– –	%	See Figure 4	–	7, 8	3	1, 14
Oscillation Frequency	f_{max}	–	–	– –	195	225 –	–	– –	MHz	See Figure 4	–	7, 8	3	1, 14

* This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

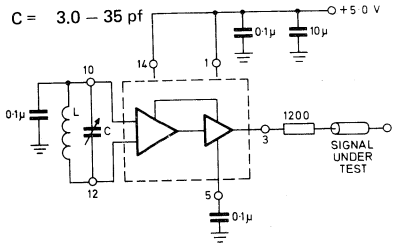


B.W. = 10kHz
Center Frequency = 100MHz

Scan Width = 50kHz/div
Vertical Scale = 10db/div

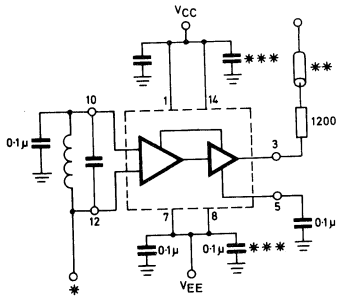
L: Micro Metal torroid #T20.13, 8 turns
#30 Enameled Copper wire.

C = 3.0 – 35 pf



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

Fig. 3 Spectral purity of signal at output



* Use high impedance probe (>1.0 Megohm must be used).

* * The 1200 -ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

* * * Bypass only that supply opposite ground.

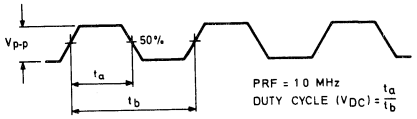


Fig. 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer. Figure 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

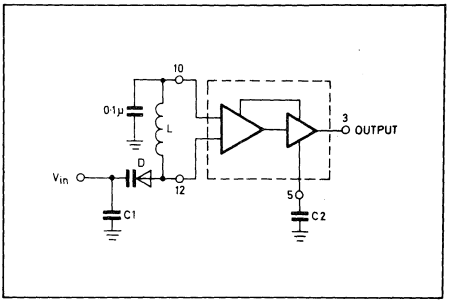
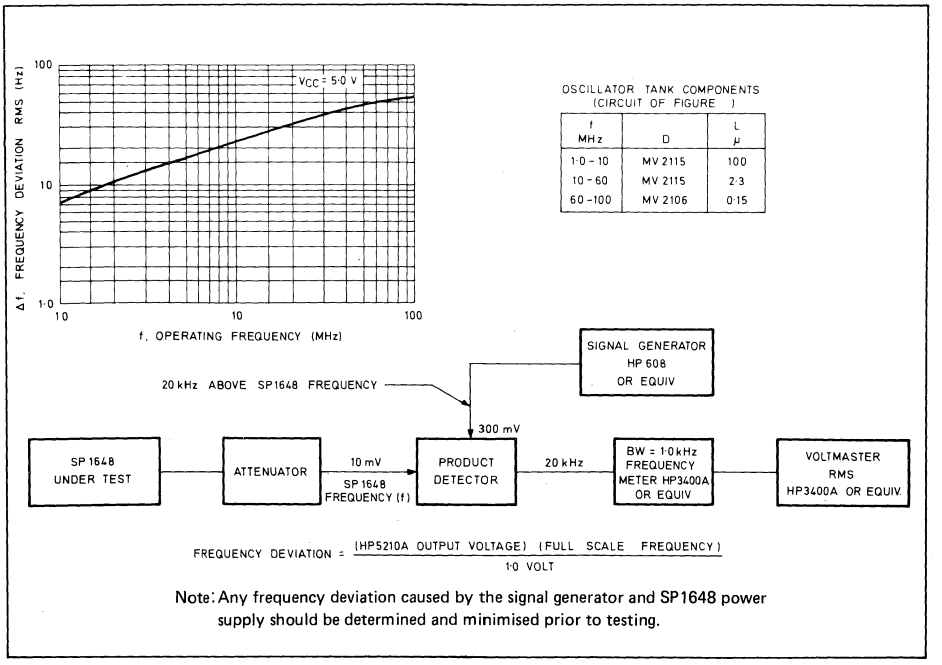


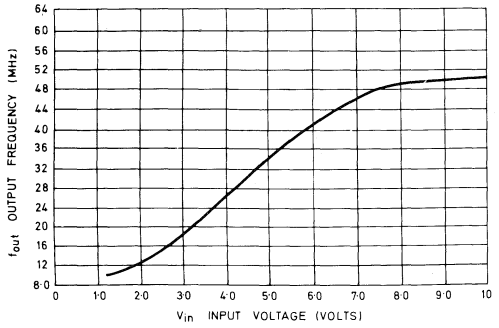
Fig. 5 The SP1648 operating in the voltage-controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 6.

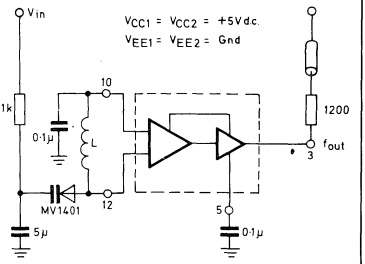


Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

Fig. 6 Frequency deviation test circuit

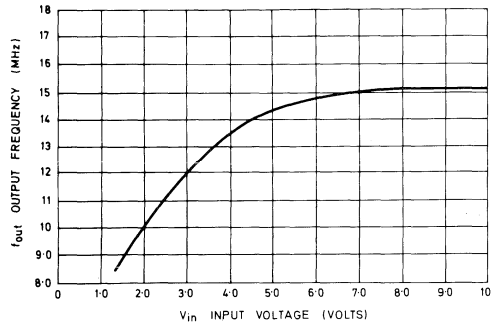


L: Micro Metal Toroidal Core #T44-10,
4 turns of No 22 copper wire.

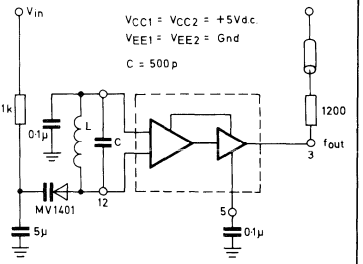


* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

Fig. 7

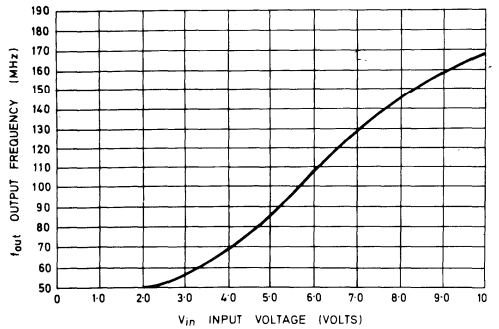


L: Micro Metal Toroidal Core #44-10,
4 turns of No. 22 copper wire.

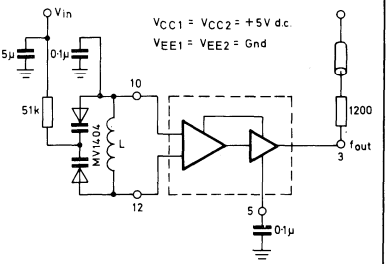


* The 1200 ohm resistor and the scope termination impedance consitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

Fig. 8



L: Micro Metal Torodial Core #T30-13,
5 turns of No. 20 copper wire.



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

Fig. 9

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\,(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used).

PLESSEY
SEMICONDUCTORS

SP1600 SERIES

ECL III

SP1650B (HIGH Z)

SP1651B (LOW Z)

DUAL A/D COMPARATOR

The SP1650 and the SP1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The SP1650 provides high impedance Darlington inputs, while the SP1651 is a lower impedance option, with higher input slew rate and higher speed capability.

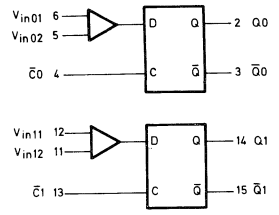
Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection and transmitters, receivers, memory translation and more.

The clock inputs ($\overline{C0}$ and $\overline{C1}$) operate from PECL III or PECL 10,000 digital levels. When $\overline{C0}$ is at a logic high level, Q0 will be at a logic high level provided that $V_{in01} > V_{in02}$ (V_{in01} is more positive than V_{in02}). $\overline{Q0}$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

FEATURES

- P_D = 275 mW typ/pkg (No Load)
- Very High Speed – 3.5 ns Delay (SP1650)
  – 2.5 ns Delay (SP1651)
- High Input Slew Rate – 350 V/μs (SP1651)
- Positive Transition Region – Input Hysterisis.

POSITIVE LOGIC



TRUTH TABLE

$\overline{CO}$	V_{in01} V_{in02}	QO_{n+1}	$\overline{QO}_{n+1}$
H	$V_{in01} > V_{in02}$	H	L
H	$V_{in01} < V_{in02}$	L	H
L	ø ø	QO_n	$\overline{QO}_n$

ø Don't Care

DG16

Fig. 1 Logic diagram of SP1651

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1658
VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with PECL III and PECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The PECL1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

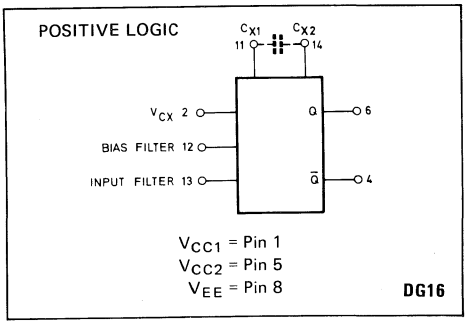


Fig. 1 Block diagram of SP1658

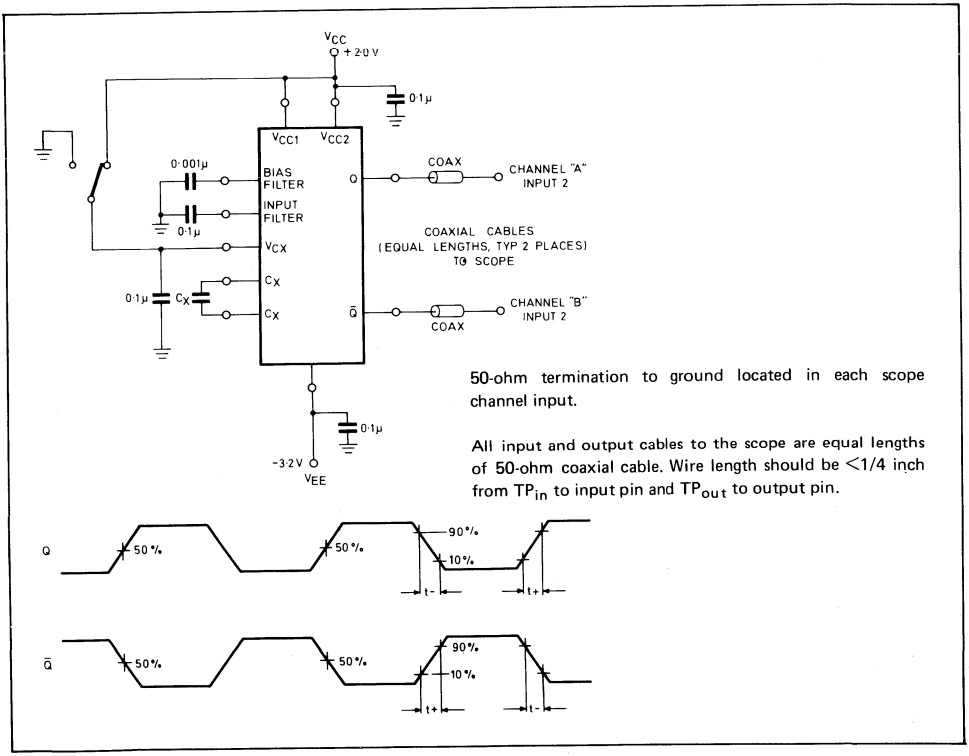


Fig. 2 AC test circuit and waveforms

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1%				
	V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
0°C	−0.0	−2.0	−1.0	+2.0	−5.2
+25°C	−0.0	−2.0	−1.0	+2.0	−5.2
+75°C	−0.0	−2.0	−1.0	+2.0	−5.2

Characteristic	Symbol	Pin Under Test	SP1658 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8 *	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
		8 * *	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
Input Current	I_{inH}	2 *	–	–	–	–	350	–	–	μAdc	2	–	–	–	8	1,5
Input Leakage Current	I_{inL}	2 *	–	–	−0.5	–	–	–	–	μAdc	–	2	–	–	8	1,5
"Q" High Output Voltage	V_{OH}	4 *	−1.000	−0.840	−0.960	–	−0.810	−0.900	−0.720	Vdc	–	–	2	–	8	1,5
		6 * *	−1.000	−0.840	−0.960	–	−0.810	−0.900	−0.720	Vdc	–	–	2	–	8	1,5
"Q" Low Output Voltage	V_{OL}	4 *	−1.870	−1.620	−1.850	–	−1.620	−1.850	−1.595	Vdc	–	–	2	–	8	1,5
		6 * *	−1.870	−1.620	−1.850	–	−1.620	−1.850	−1.595	Vdc	–	–	2	–	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	Gnd	V_{ILA} +1.0V	V_{IHA} +2.0V	V_{EE} −3.2V	V_{CC} +2.0V
	t†	6	–	2.5	–	1.6	2.5	–	2.7	ns	–	11,14	–	–	2	8	1,5
	t−	6	–	2.5	–	1.4	2.5	–	2.7		–		–	–	2		
	t+	6	–	4.6	–	3.7	4.6	–	4.8		–		–	2	–		
	t−	6	–	4.2	–	2.4	4.2	–	4.4		–		–	–	2		
Rise Time (10% to 90%) Fall Time (10% to 90%)	t+	6	–	8.5	–	5.7	8.5	–	8.7		–		2	–	–		
	t−	6	–	8.5	–	5.9	8.5	–	8.7		–		2	–	–		
Oscillator Frequency	f_{osc1}	–	130	–	130	155	175	110	–	MHz	–	11,14	–	–	2	8	1,5
	f_{osc2}	–	–	–	78	90	100	–	–	MHz	11,14	–	–	–	2	8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	–	–	–	–	11,14	–	–	–	–	8	1,5

* Germanium diode (0.4 drop) forward biased from 11 to 14 (11 —▷|— 14).

* * Germanium diode (0.4 drop) forward biased from 14 to 11 (11 —|◁— 14).

†TR = $\frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ \text{V}}$

C1 = 0.01 μF connected from pin 12 to Gnd.
C2 = 0.001 μF connected from pin 13 to Gnd.
C_{X1} = 10 pF connected from pin 11 to pin 14.
C_{X2} = 5 pF connected from pin 11 to pin 14.

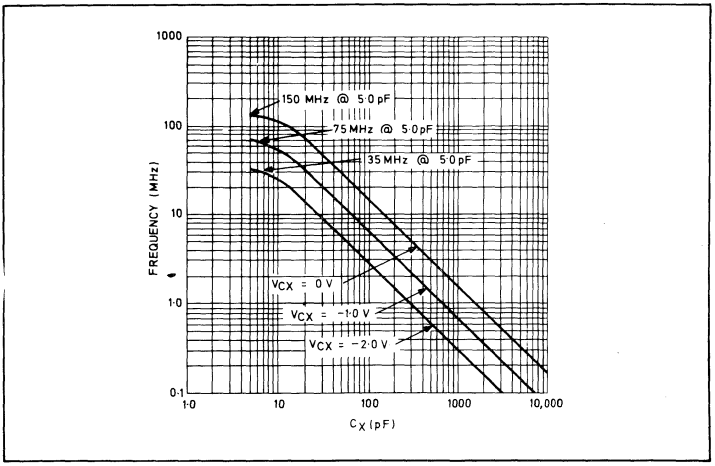


Fig. 3 Output frequency v capacitance for three values of input voltage

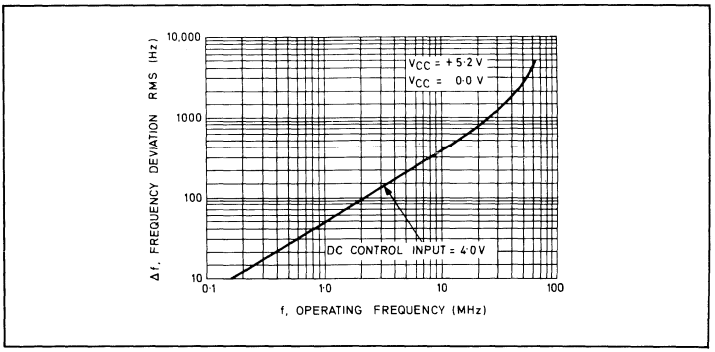


Fig. 4 RMS noise deviation v operating frequency

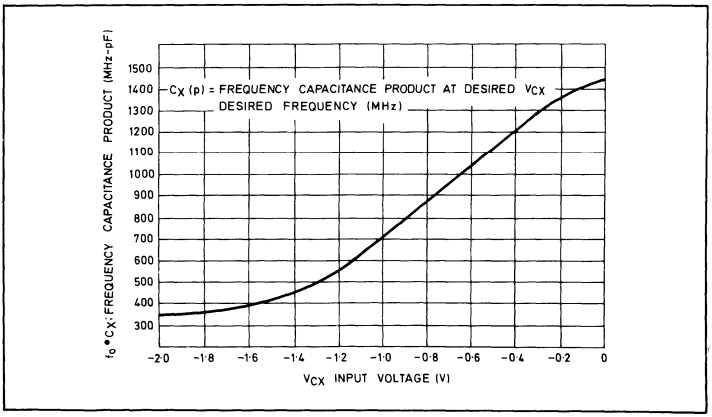


Fig. 5 Frequency-capacitance product v control voltage V_{CX}

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1660B (HIGH Z)
SP1661B (LOW Z)
DUAL 4-INPUT OR/NOR GATE

SP1660B provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (0°C to +75°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

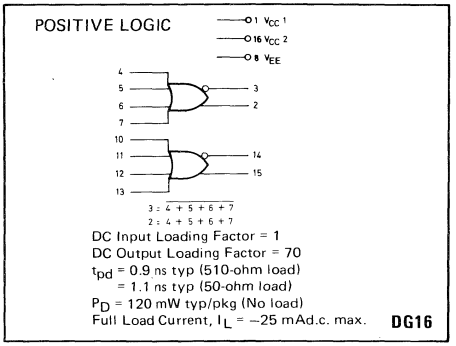


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- MECL/PECL II and MECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	55°C to +150°C
Junction operating temp.	< +125°C

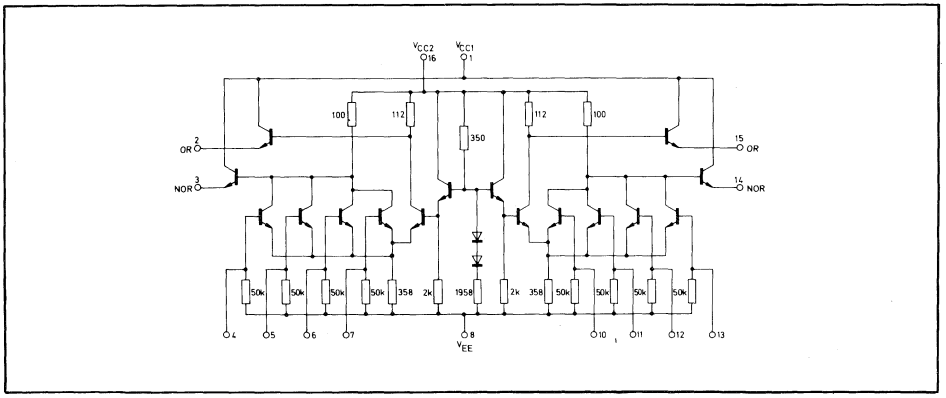


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 14A2CB or equivalent) or a transverse air flow greater than 500 linear ft/min should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to −2.0 Vd.c.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1660B Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
			0°C		+25°C		+75°C								
			Min	Max	Min	Max	Min	Max	Units	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	OV
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	−1.020	–	−0.980	–	−0.920	–	V	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	−1.615	–	−1.600	–	−1.575	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	1.1	1.7	1.1	1.7	1.2	1.9			2	–	–		
	t_{4+2+}	2	1.0	1.5	1.0	1.5	1.1	1.7			2	–	–		
	t_{4-3+}	3	1.0	1.5	1.0	1.5	1.1	1.7			3	–	–		
Rise Time	t_{3+}	3	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

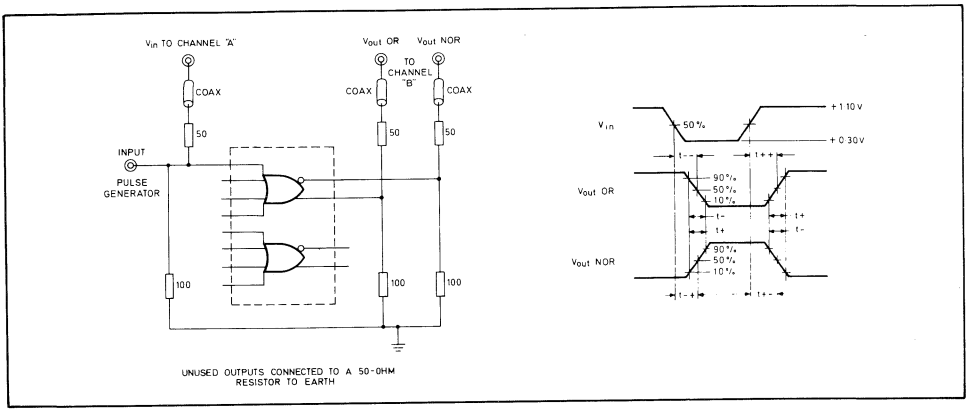


Fig. 3 Switching time test circuit and wave forms at +25°C

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1662B (HIGH Z)
SP1663B (LOW Z)
QUAD 2-INPUT NOR GATE

The SP1662B comprises four 2-input NOR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (0°C to +75°C).

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

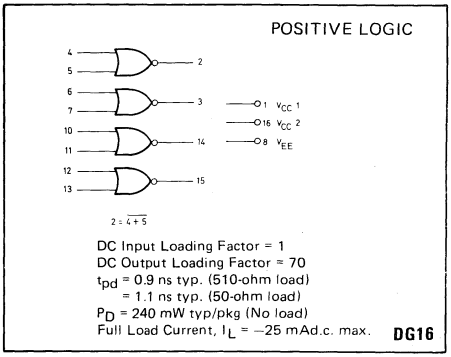


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- MECL/PECL II and MECL 10000–Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\|V_{CC} - V_{EE}\|$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to +150°C
Junction operating temp.	< +125°C

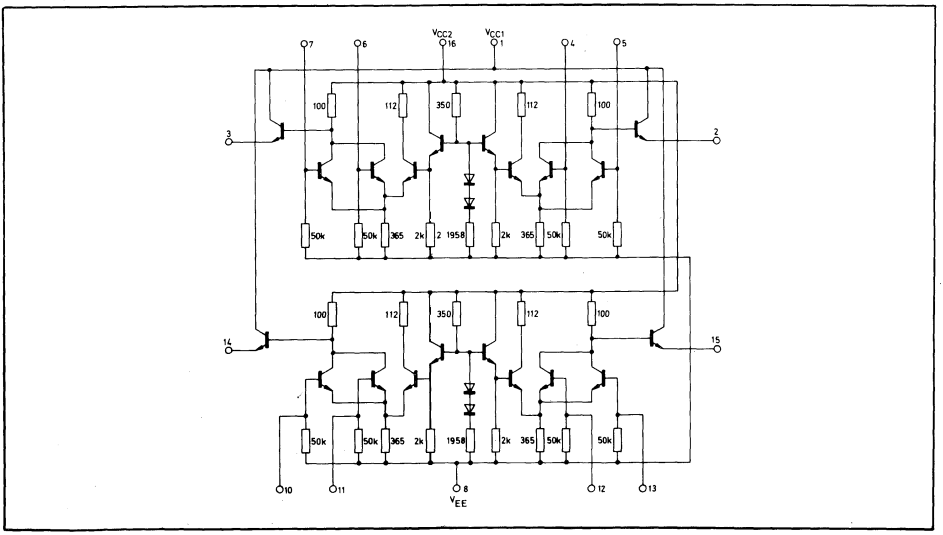


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear ft/min should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1662B Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
			0°C		+25°C		+75°C								
			Min	Max	Min	Max	Min	Max	Units	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	OV
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
Logic 1 Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	4	–	–	8	1,16
		2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	5	–	–	8	1,16
Logic 0 Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	4	–	–	–	8	1,16
		2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	5	–	–	–	8	1,16
Logic 1 Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	–	–	4	8	1,16
		2	−1.020	–	−0.980	–	−0.920	–	V	–	–	–	5	8	1,16
Logic 0 Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	–	–	4	–	8	1,16
		2	–	−1.615	–	−1.600	–	−1.575	V	–	–	5	–	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			−3.2V	−2.0V
Propagation Delay	t_{4-2-}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	–	–	8	1,16
	t_{4+2-}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3	ns	4	2	–	–	8	1,16

Individually test each input applying V_{IH} or V_{IL} to input under test.

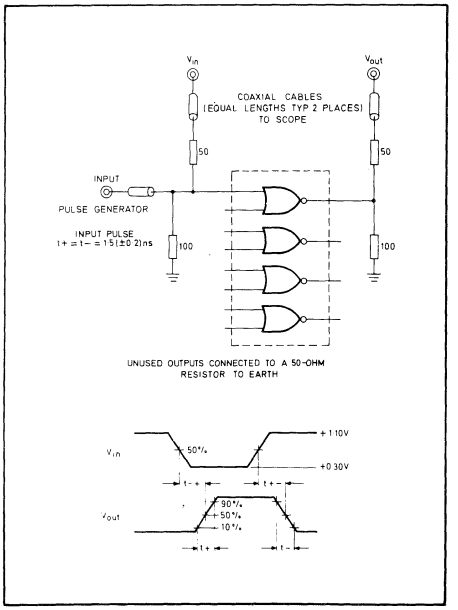


Fig. 3 Switching time test circuit and wave forms at +25°C

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1664B (HIGH Z)
SP1665B (LOW Z)
QUAD 2-INPUT OR GATE

The SP1664B comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (0°C to +75°C).

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

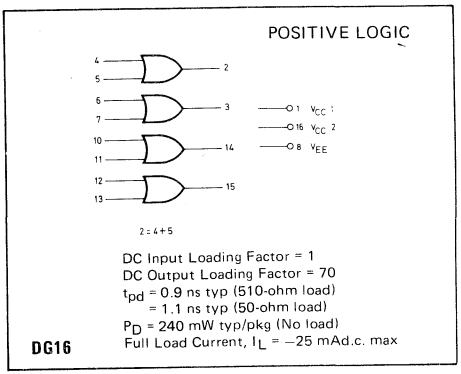


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- MECL/PECL II and MECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\|V_{CC} - V_{EE}\|$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to + 150°C
Junction operating temp.	< +125°C

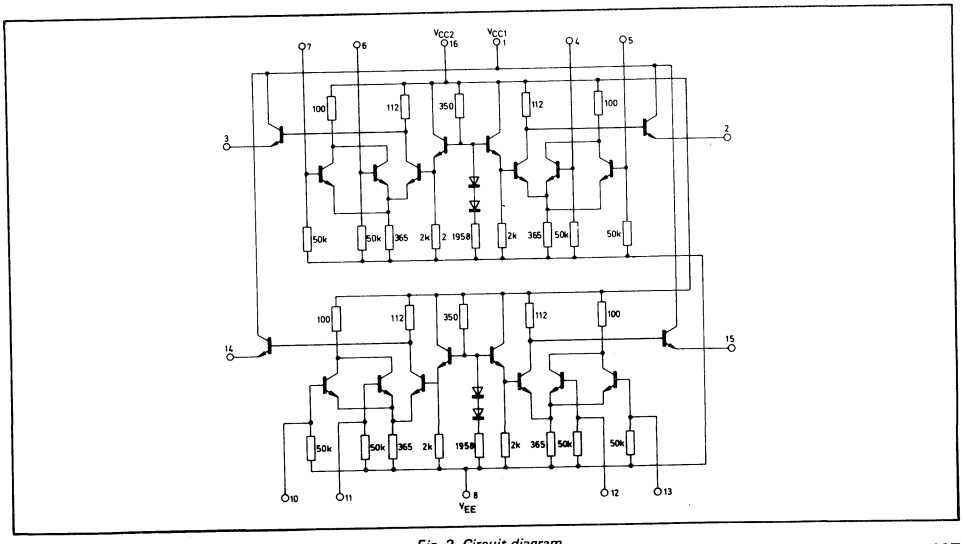


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 14A2CB or equivalent) or a transverse air flow greater than 500 linear ft/min should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to −2.0 Vd.c.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1664B Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
			0°C		+25°C		+75°C								
			Min	Max	Min	Max	Min	Max	Units	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	OV
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	4	–	–	–	8	1,16
		2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	–	4	–	–	8	1,16
		2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	–	4	–	8	1,16
		2	−1.020	–	−0.980	–	−0.920	–	V	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	–	–	–	4	8	1,16
		2	–	−1.615	–	−1.600	–	−1.575	V	–	–	–	5	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Propagation Delay	t_{4+2-}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4	2	–	–	8	1,16
	t_{4-2+}	2	1.1	1.7	1.1	1.7	1.2	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	1.5	2.1	1.5	2.1	1.6	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	1.4	2.1	1.4	2.1	1.5	2.3	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

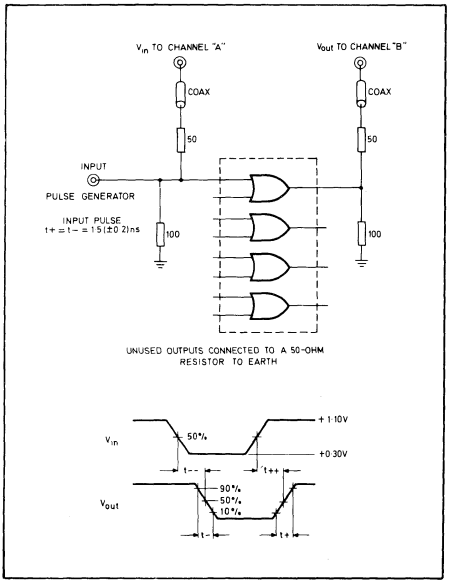


Fig. 3 Switching time test circuit and wave forms at +25°C

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1666B (HIGH Z)
SP1667B (LOW Z)
DUAL CLOCKED R-S FLIP-FLOP

Two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage.

The device is useful as a high-speed dual storage element.

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	0
0	1	1	0
1	1	1	N.D.

ϕ = Don't care
N.D. = Not Defined

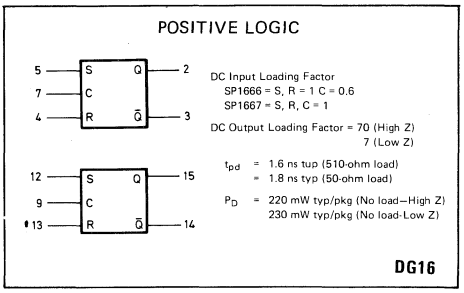


Fig. 1 Logic diagram of SP1666/1667

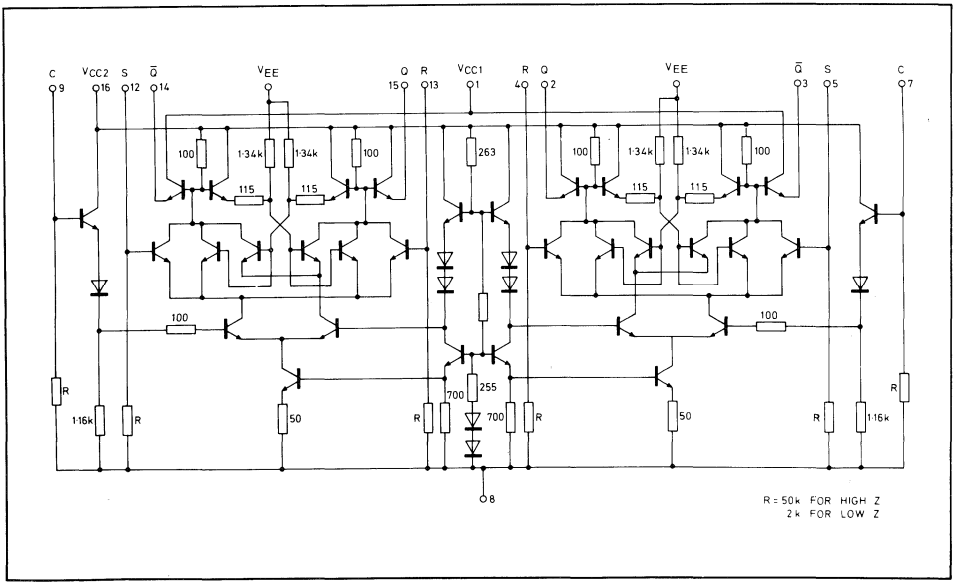


Fig. 2 Circuit diagram

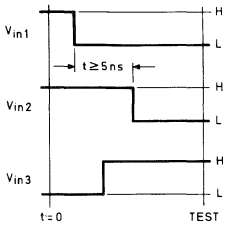
ELECTRICAL CHARACTERISTICS

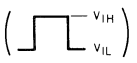
This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test / @ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1666/SP1667 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E(Hi-Z) ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
	I_E(Lo-Z) ①	8	–	–	–	60	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current (Hi-Z)	$I_{in\ H}$	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	12	–	–	0.500	–	–	–	μAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	μAdc	–	9,13	–	–	8	1,16
Input Current (Lo-Z)	$I_{in\ H}$	12	–	–	–	3.1	–	–	mAdc	9,12	–	–	–	8	1,16
		9,13	–	–	–	3.1	–	–	mAdc	9,13	–	–	–	8	1,16
	$I_{in\ L}$	12	–	–	1.300	–	–	–	mAdc	–	12	–	–	8	1,16
		9,13	–	–	1.300	–	–	–	mAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	13	–	–	8	1,16
		15 ③	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	−1.870	−1.635	−1,850	−1.620	−1.830	−1.595	Vdc	–	12	–	–	8	1,16
		15 ⑤	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	14 ④	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	12	–	–	8	1,16
		14 ⑤	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	14 ②	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	13	–	–	8	1,16
		14 ③	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	−1.020	–	−0.980	–	−0.920	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑥	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	13	12	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OHA}	14 ⑥	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	13	12	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	−1.615	–	−1.600	–	−1.575	Vdc	–	13	9	–	8	1,16
Switching Times (50Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Clock Input	t_{9+15+}	15	1.0	2.5	1.0	2.5	1.1	2.7	ns	9	15	–	–	8	1,16
	t_{9+15-}	15	↓	↓	↓	↓	↓	↓		↓	15	–	–	↓	↓
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.3	1.0	2.3	1.1	2.6	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.3	1.0	2.3	1.1	2.6	ns	12	14	–	–	8	1,16
Reset Input	t_{13+15-}	14	1.0	2.3	1.0	2.3	1.1	2.6	ns	13	14	–	–	8	1,16
	t_{13+14+}	15	1.0	2.3	1.0	2.3	1.1	2.6	ns	13	15	–	–	8	1,16
Rise Time	t+	14,15	0.8	2.5	0.8	2.5	0.9	2.8	ns	9	14,15	–	–	8	1,16
Fall Time	t−	14,15	0.5	2.2	0.5	2.2	0.5	2.5	ns	9	14,15	–	–	8	1,16

(1) I_E is measured with no output pull-down resistors.





(2) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} ro S (V_{IH} to V_{IL})

(3) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IL} to V_{IL})

(4) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(5) Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(6) Apply V_{in3} to C, (V_{IH} to V_{IL})

(7) Apply V_{in3} to S (V_{IH} to V_{IL})

Fig. 3 Notes referred to in electrical characterstics

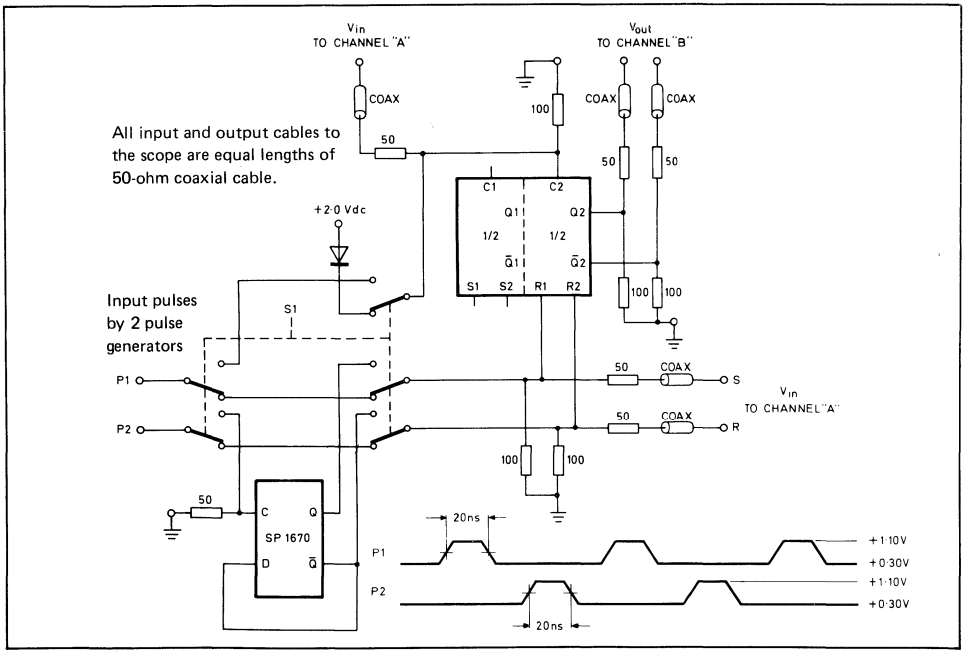


Fig. 4 Switching time test circuit

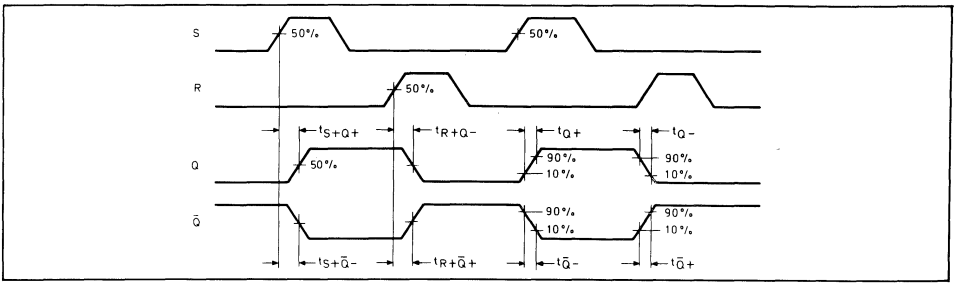


Fig. 5 Switching time waveforms (set/reset to Q/$\bar{Q}$, switch S1 in position shown in Fig. 4)

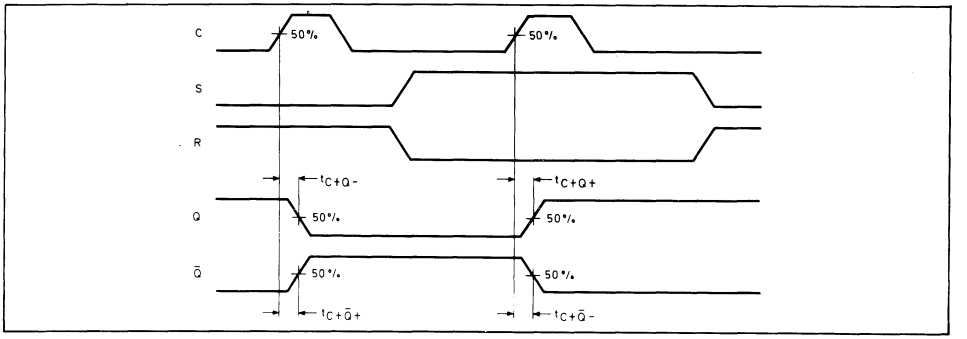


Fig. 6 Switching time waveforms (clock to Q/$\bar{Q}$, switch S1 in opposite position to that shown in Fig. 4)

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1668B (HIGH Z)
SP1669B (LOW Z)
DUAL CLOCKED LATCH

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the date (D) input.

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ø	0	Q_n
1	0	ø	0	1
0	1	ø	0	0
1	1	ø	0	**
ø	ø	0	1	0

** Output stage not defined
ø Don't care

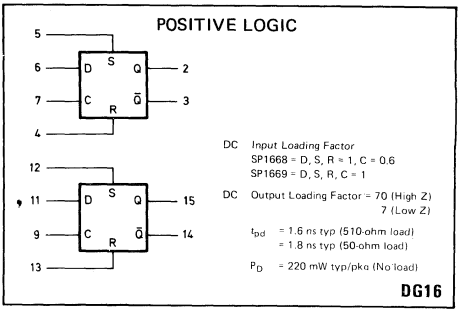


Fig. 1 Logic diagram of SP1668/1669

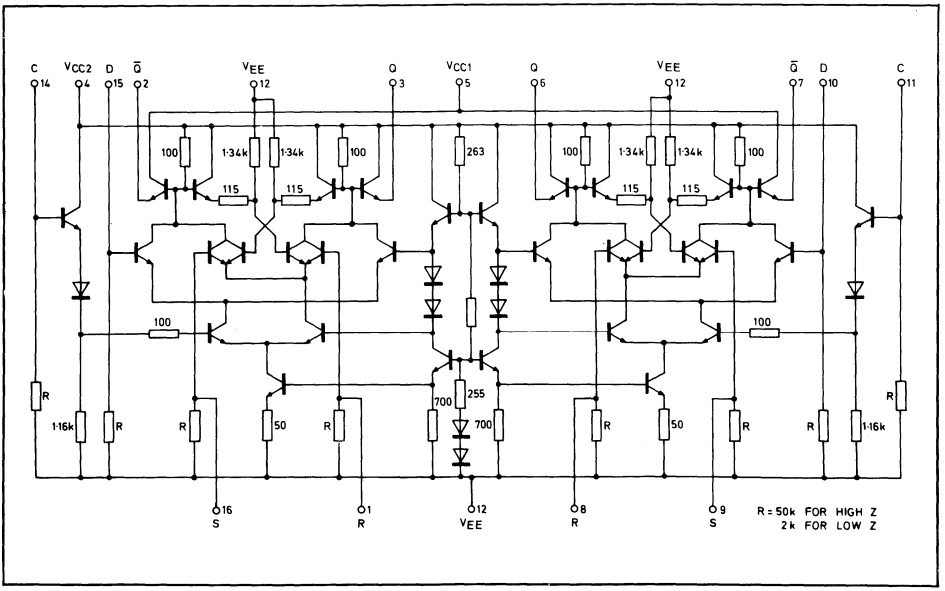


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

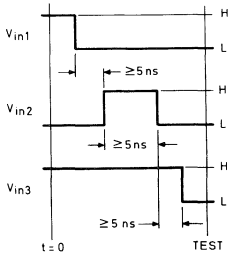
This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1668 /SP1669 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E (Hi-Z) ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
	I_E (Lo-Z) ①	8	–	–	–	60	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current (Hi-Z)	I_{in} H	11,12,13 ②	–	–	–	0.370	–	–	mAdc	11,12,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{in} L	11,12,13 ②	–	–	0.500	–	–	–	μAdc	–	11,12,13	–	–	8	1,16
		9	–	–	0.500	–	–	–	μAdc	–	9	–	–	8	1,16
Input Current (Lo-Z)	I_{in} H	11,12,13 ②	–	–	–	3.2	–	–	mAdc	11,12,13	–	–	–	8	1,16
		9	–	–	–	3.1	–	–	mAdc	9	–	–	–	8	1,16
	I_{in} L	11,12,13 ②	–	–	1.300	–	–	–	mAdc	–	11,12,13	–	–	8	1,16
		9	–	–	1.300	–	–	–	mAdc	–	9	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ③	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	13	–	–	8	1,16
		15 ④	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	14 ⑤	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	12	–	–	8	1,16
		14 ⑥	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	14 ⑤	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	12	–	–	8	1,16
		14 ⑥	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	14 ③	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	13	–	–	8	1,16
		14 ④	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	↓	–	↓	–	↓	–	↓	–	–	11	–	↓	↓
		15 ⑤		–		–		–		11	–	9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	13	12	8	1,16
		15 ⑥	–	↓	–	↓	–	↓	↓	–	–	–	11	↓	↓
		15 ③	–		–		–			–	11	9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OHA}	14	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	13	12	8	1,16
		14 ⑥	↓	–	↓	–	↓	–	↓	–	–	–	11	↓	↓
		14 ③		–		–		–		–	11	9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	14	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	↓	–	↓	–	↓	↓	–	11	–	–	↓	↓
		14 ⑤	–		–		–			–	–	9	–		
Switching Times (50Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Clock Input	t_{9+15+}	15	1.0	2.5	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9+15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Rise Time	t_+	14,15	0.8	2.5	0.9	2.5	0.9	2.8	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.2	0.5	2.2	0.5	2.5	ns	9	14,15	–	–	8	1,16
Set Input	t_{12+15+}	15	1.0	2.3	1.1	2.3	1.1	2.6	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.3	1.1	2.3	1.1	2.6	ns	12	14	–	–	8	1,16
Reset Input	t_{13+14+}	14	1.0	2.3	1.1	2.3	1.1	2.6	ns	13	14	–	–	8	1,16
	t_{13+15-}	15	1.0	2.3	1.1	2.3	1.1	2.6	ns	13	15	–	–	8	1,16

(1) I_E is measured with no output pulldown resistors.

(2) Test voltage applied to pin under test.



(3) Apply V_{in1} to S (V_{IH} to V_{IL}).

(4) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

(5) Apply V_{in1} to R (V_{IH} to V_{IL})

(6) Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})

(7) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})

Fig. 3 Notes referred to in electrical characteristics

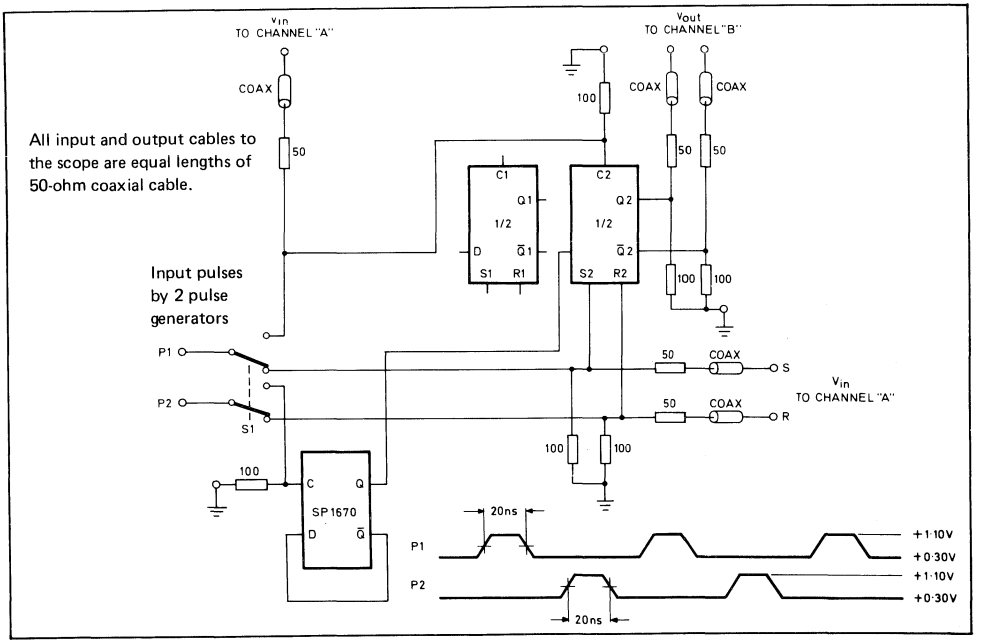


Fig. 4 Switching time test circuit

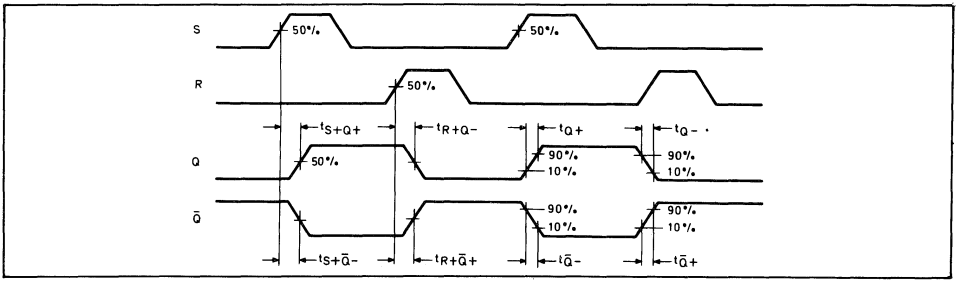


Fig. 5 Switching time waveforms (set/reset to Q/$\bar{Q}$, switch S1 in position shown in Fig. 3)

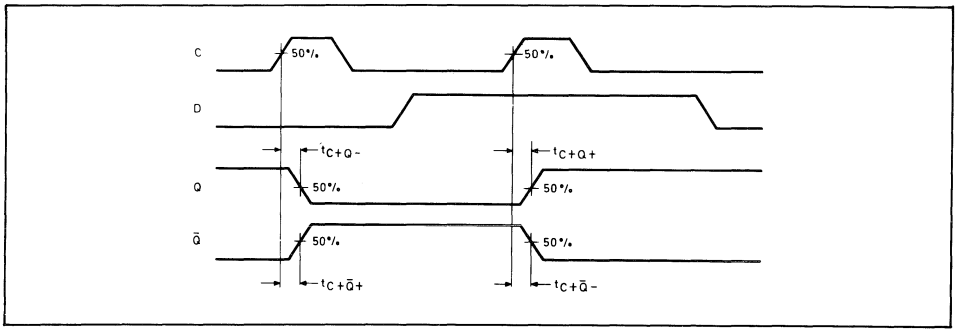


Fig. 6 Switching time waveforms (clock to Q/$\bar{Q}$, switch S1 in position opposite to that shown in Fig. 3

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1670B (HIGH Z)
SP1671B (LOW Z)
MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670B is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670B relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

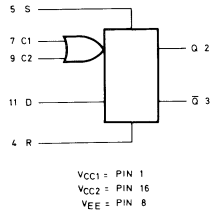
When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state, the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



DC Input Loading Factor = C1, C2 = 0.67 D = 0.75 R,S = 1.5
DC Output Loading Factor = 70
Power Dissipation = 200 mW typical (No Load)
f_{tog} = 350 MHz typ

DG16

Fig. 1 Logic diagram

FEATURES

- Toggle Frequency > 300 MHz
- MECL/PECL II and MECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

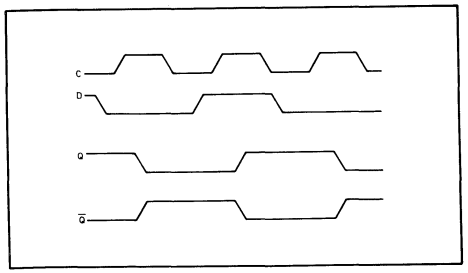


Fig. 2 Timing diagram

TRUTH TABLE				
R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↓	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↓	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to +150°C
Junction operating temp.	<+125°C

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+ 25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+ 75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1670B Test Limits 0°C Min	0°C Max	+ 25°C Min	+ 25°C Max	+ 75°C Min	+ 75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	OV
Power Supply Drain Current	I_E	–	–	–	–	48	–	–	mA	9,7	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	µA	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\ L}$	4	–	–	0.5	–	–	–	µA	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						−3.2 V				+2.0 V
Clock to Output Delay (See Figure 5)	t_{9+2+}	9,2	1.0	2.5	1.1	2.5	1.1	2.7	ns	–	–	–	–	8	–	–	–	1,16
	t_{9-2-}	9,2								–	–	–	–		–	–	–	
	t_{9+3-}	9,3								–	–	–	–		–	–	–	
	t_{9-3+}	9,3								–	–	–	–		–	–	–	
Set to Output Delay (See Figure 6)	t_{5+2+}	5,2								–	–	–	–		–	–	–	
	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay (See Figure 6)	t_{4+2-}	4,2								–	–	–	–		–	–	–	
	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	t_{2+}, t_{3+}	2,3	0.9	2.5	1.0	2.5	1.0 *	2.7		–	–	–	–		–	–	–	
Fall Time (See Figure 6)	t_{2-}, t_{3-}	2,3	0.5	1.9	0.6	1.9	0.6	2.1		–	–	–	–		–	–	–	
Set Up Time (See Figure 7)	$t_{s^{"1"}}$	2	–	–	–	0.4	–	–		–	2	–	–		–	–	–	
	$t_{s^{"0"}}$	2	–	–	–	0.5	–	–		–	2	–	–		–	–	–	
Hold Time (See Figure 7)	$t_{H^{"1"}}$	2	–	–	–	0.3	–	–		–	2	–	–		–	–	–	
	$t_{H^{"0"}}$	2	–	–	–	0.5	–	–		–	2	–	–		–	–	–	
Toggle Frequency (See Figure 8)	f_{Tog}	2	270	–	300	–	270	–	MHz	–	–	–	–		–	–	–	–

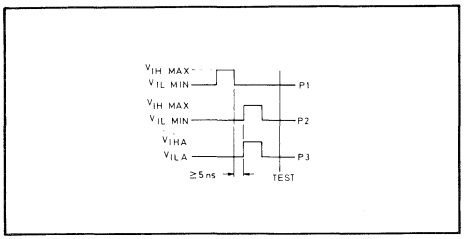


Fig. 3 Static test pulses

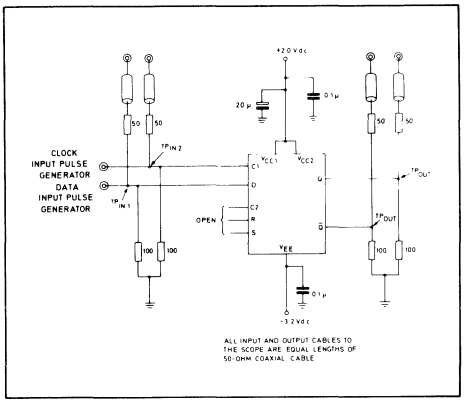


Fig. 4 Propagation delay test circuit

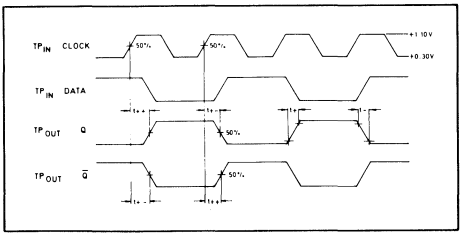


Fig. 5 Clock delay waveforms at +25°C

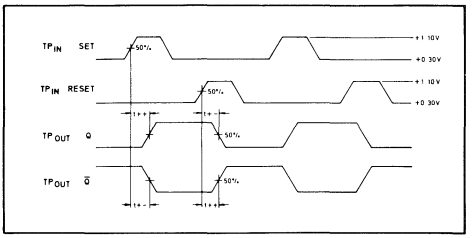


Fig. 6 Set/reset delay waveform at +25°C

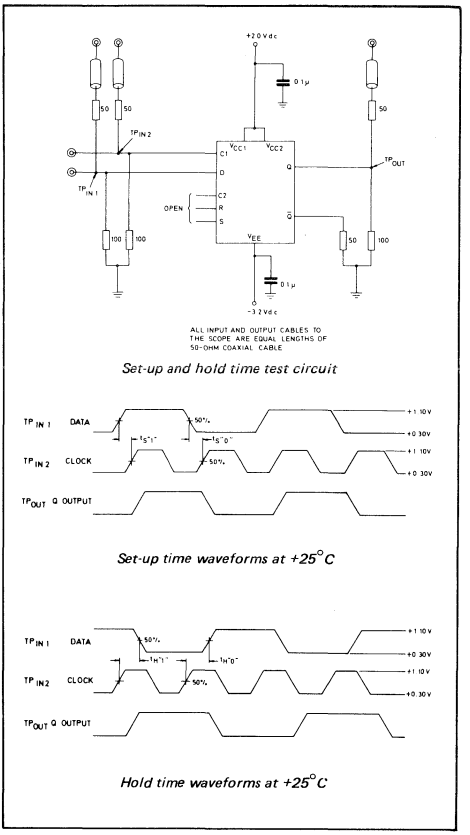


Fig. 7 Set-up and hold time test circuit

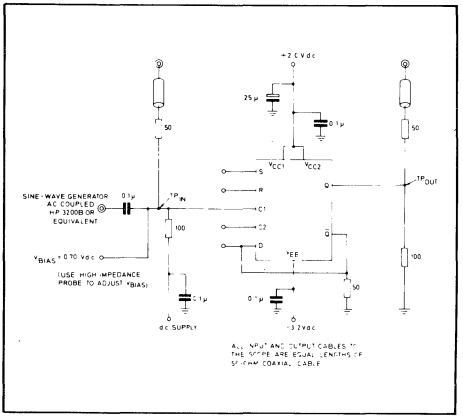


Fig. 8 Toggle frequency test circuit

OPERATING NOTES

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

V_{Bias} is defined by the test circuit Fig.8 and by the waveform in Fig.9.

Figures 10 and 11 illustrate minimum clock pulse width recommended for reliable operation of the SP1670B.

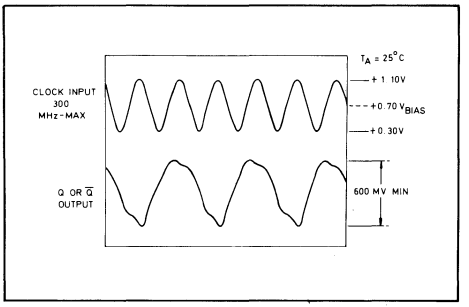


Fig. 9 Toggle frequency waveforms

The maximum toggle frequency of the SP1670B has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts.
   OR
2. The device ceases to toggle (divide by two).

Temperature	0°C	+25°C	+75°C
V_{Bias}	+0.675V	+0.700V	+0.750V

Table 1 Variation of V_{Bias} with temperature

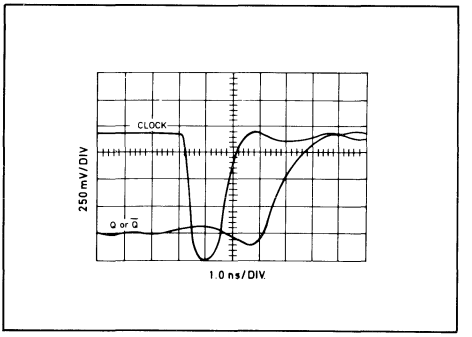


Fig. 10 Minimum 'downtime' to clock output load = 50Ω

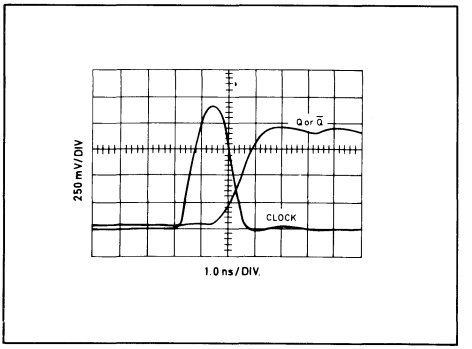


Fig. 11 Minimum 'up time' to clock output load = 50Ω

Operation of the Master-Slave Type D Flip-Flop

In the circuit of Figure 14 assume that initially Q, C, R, S and D are at 0 levels and that $\overline{Q}$ is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7, and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turns on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the $\overline{Q}$ output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

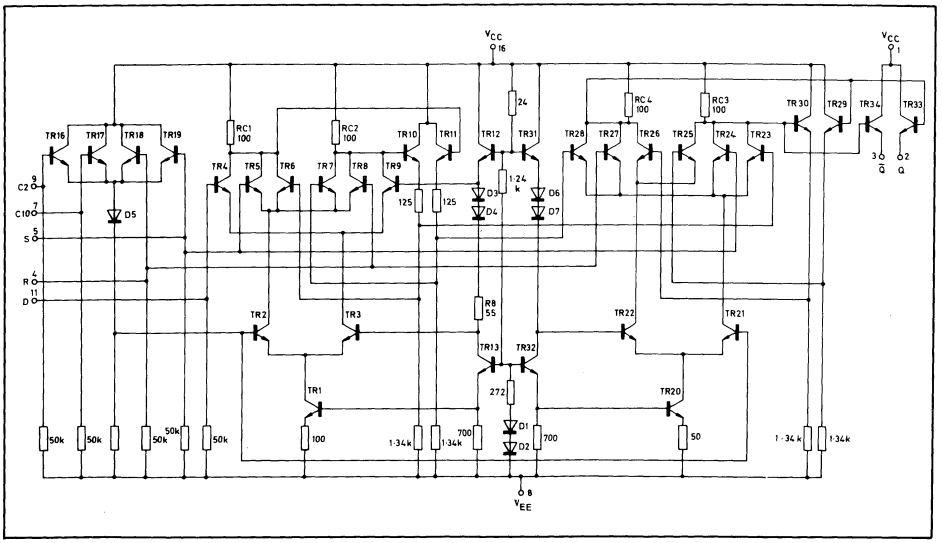


Fig. 12 SP1670 circuit diagram

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1672B (HIGH Z)
SP1673B (LOW Z)
TRIPLE 2-INPUT EXCLUSIVE-OR GATE

This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (0° to +75°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

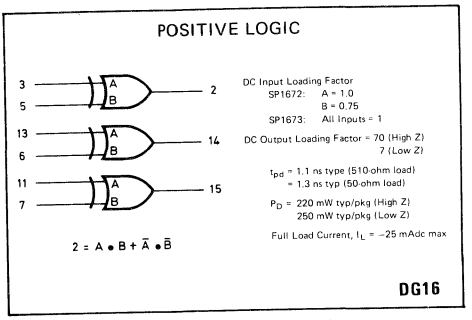


Fig. 1 Logic diagram of SP1672/1673

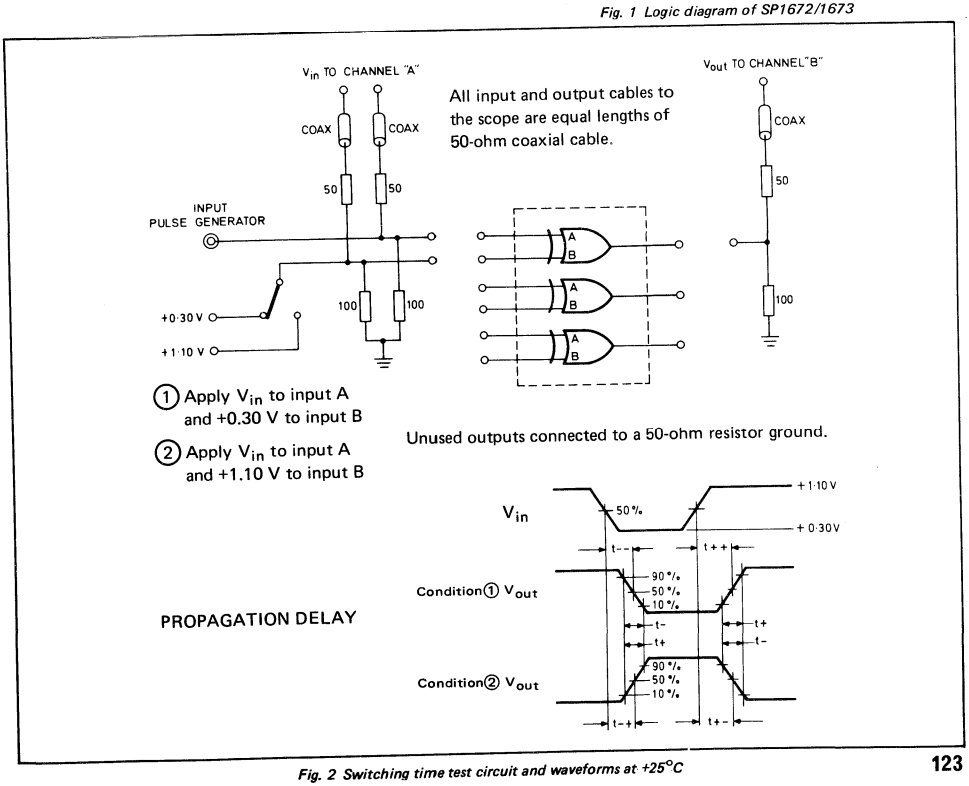


Fig. 2 Switching time test circuit and waveforms at +25°C

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Outputs are tested with a 50-ohm resistor to −2.0V.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1672 /SP1673 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E (Hi-Z)	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
	I_E (Lo-Z)	8	–	–	–	70	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current (Hi-Z)	$I_{in\ H}$	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0,75 $I_{in\ H}$	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Input Current (Lo-Z)	$I_{in\ H}$	*	–	–	–	3.1	–	–	mAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	1.3	–	–	–	mAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	3	5	–	–	8	1,16
		2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	5	3	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	3,5	–	–	–	8	1,16
		2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	3,5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	3	5	8	1,16
		2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	3,5	–	8	1,16
		2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	–	3,5	8	1,16
Switching Time (50Ω Load) Propagation Delay			Typ	Max	Typ	Max	Typ	Max				Pulse In	Pulse Out	−3.2V	+2.0V
	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	1.2	1.8	1.3	1.8	1.5	2.2	ns	–	–	↓	↓	↓	↓
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3	ns	–	–				
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3	ns	–	–				
	t_{5+2+}	2	1.7	2.3	1.7	2.3	1.9	2.7	ns	–	–	5			
	t_{5-2+}	2	↓	↓	↓	↓	↓	↓	ns	–	–	↓			
	t_{5+2-}	2								–	–				
	t_{5-2-}	2								–	–				
Rise Time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	–	–	3	2	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1674B (HIGH Z)
SP1675B (LOW Z)
TRIPLE 2-INPUT EXCLUSIVE-NOR GATE

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (0° to +75°). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

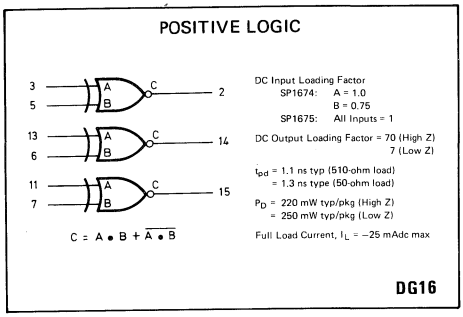


Fig. 1 Logic diagram of SP1674/1675

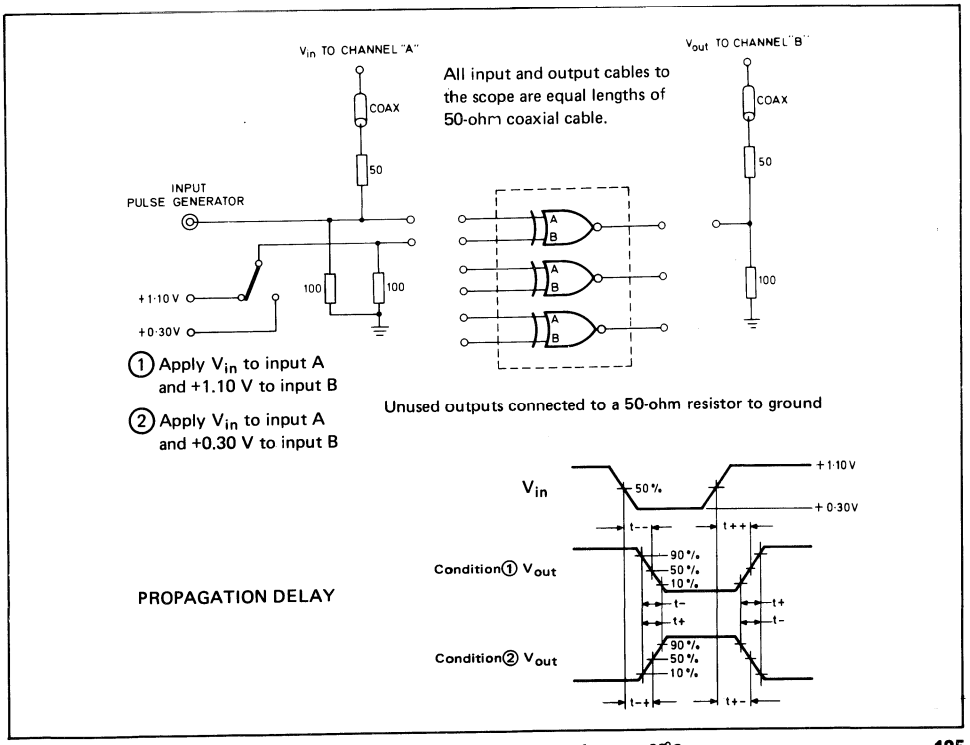


Fig. 2 Switching time test circuit and waveforms at +25°C

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board. Outputs are tested with a 50-ohm resistor to −2.0 V.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1674/SP1675 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75° Min	+75° Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E (Hi-Z)	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
	I_E (Lo-Z)	8	–	–	–	70	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current (Hi-Z)	I_{in} H	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 I_{in} H	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	I_{in} L	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Input Current (Lo-Z)	I_{in} H	*	–	–	–	3.1	–	–	mAdc	*	–	–	–	8	1,16
	I_{in} L	*	–	–	1.3	–	–	–	mAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	3,5	–	–	–	8	1,16
		2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	3,5	–	–	–	8	1,16
		2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	3.5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	3,5	–	8	1,16
		2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Treshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	3	5	8	1,16
		2	–	−1.615	–	−1.600	–	−1,575	Vdc	–	–	5	3	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max					Pulse In	Pulse Out	−3.2V	+2.0V
Propagation Delay	t_{3+2+}	2	1.3	1.8	1.3	1.8	1.5	2.2	ns	–	–		3	2	8	1,16
	t_{3-2+}	2	1.3	1.8	1.3	1.8	1.5	2.2		–	–					
	t_{3+2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		–	–					
	t_{3-2-}	2	1.4	1.9	1.4	1.9	1.6	2.3		–	–					
	t_{5+2+}	2	1.7	2.3	1.7	2.3	1.9	2.7		–	–		5			
	t_{5-2+}	2								–	–					
	t_{5+2-}	2								–	–					
	t_{5-2-}	2								–	–					
Rise Time	t_{2+}	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	–	–		3	2	8	1,16
Fall Time	t_{2-}	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	–	–		3	2	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test.

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1690B
UHF PRESCALER TYPE D FLIP-FLOP

The SP1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary $\overline{Q}$ and Q outputs. It is a higher frequency replacement for the SP1670 (350 MHz) D flip-flop. No set or reset inputs are provided and an extra data input is provided on pin 11.

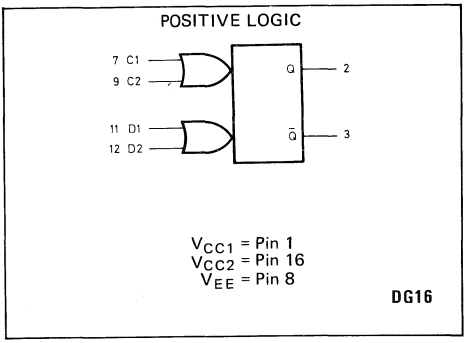
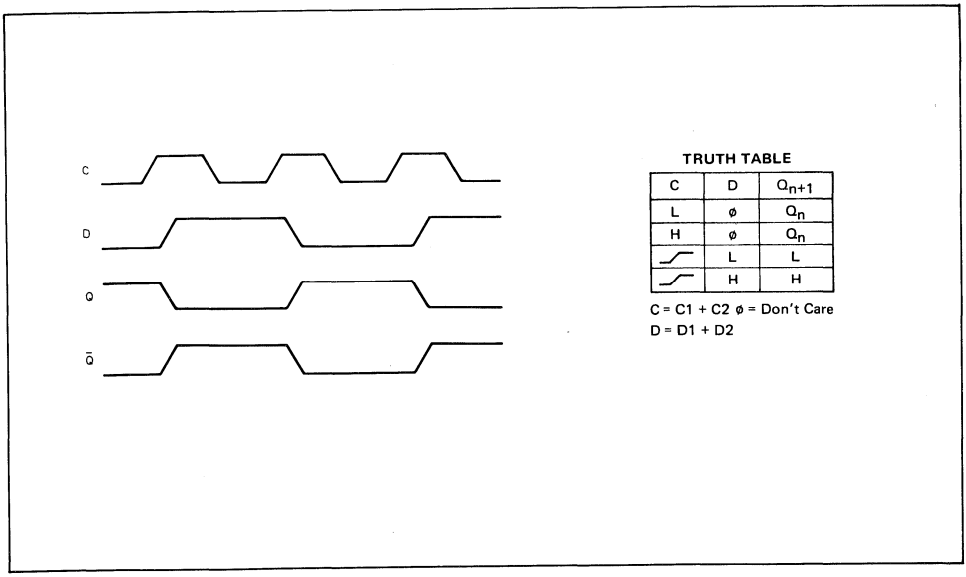


Fig. 1 Logic diagram of SP1690

FEATURES

- P_D = 200 mW typ/pkg (No Load)
- f_{tog} = 500 MHz min



TRUTH TABLE

C	D	Q_{n+1}
L	ø	Q_n
H	ø	Q_n
⌐	L	L
⌐	H	H

C = C1 + C2 ø = Don't Care
D = D1 + D2

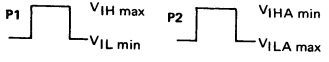
Fig. 2 Timing diagram

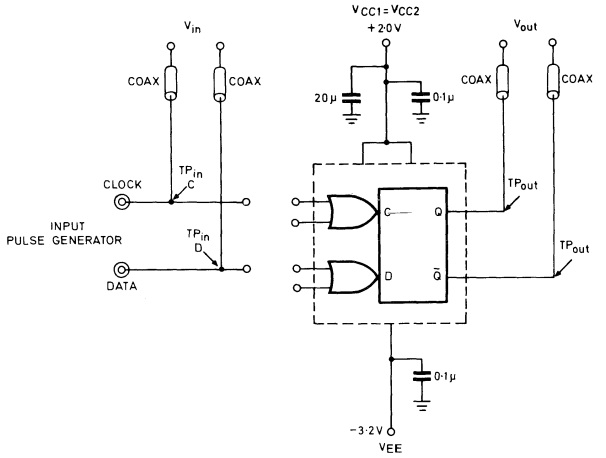
ELECTRICAL CHARACTERISTICS

Each PECL III series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1690 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	P1	P2	Gnd
Power Supply Drain Current	I_E	8	–	–	–	59	–	–	mAdc	7,9,11,12	–	–	–	8	–	–	1,16
Input Current	I_{in} H	7	–	–	–	250	–	–	µAdc	7	–	–	–	8	–	–	1,16
		11	–	–	–	270	–	–	µAdc	11	–	–	–	8	–	–	1,16
	I_{in} L	7	–	–	0.5	–	–	–	µAdc	–	7	–	–	8	–	–	1,16
		11	–	–	0.5	–	–	–	µAdc	–	11	–	–	8	–	–	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	11	–	–	–	8	7	–	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	11	–	–	8	7	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	11	–	–	–	8	–	7	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	11	–	–	8	–	7	1,16
Switching Parameters					Min	Typ	Max							−3.2 Vdc			+2.0 Vdc
Clock to Output Delay	t_{7+2+}	2	–	–	–	1.5	–	–	–	ns	–	–	–	–	8	–	–	1,16
	t_{9+2+}		–	–	–	1.5	–	–	–		–	–	–	–		–	–	
Output Rise Time	t_+		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Fall Time	t_-		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Setup Time	t_{setup} H		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
	t_{setup} L		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Hold Time	t_{hold} H		–	–	–	0.2	–	–	–		–	–	–	–		–	–	
	t_{hold} L		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Toggle Frequency	t_{tog}	2	–	–	500	540	–	–	–	MHz	–	–	–	–	8	–	–	1,16





All input and output cables to the scope are equal lengths of 50-ohm coaxial cable

50-ohm termination to ground located in each scope channel input

Fig. 3 Propagation delay test circuit

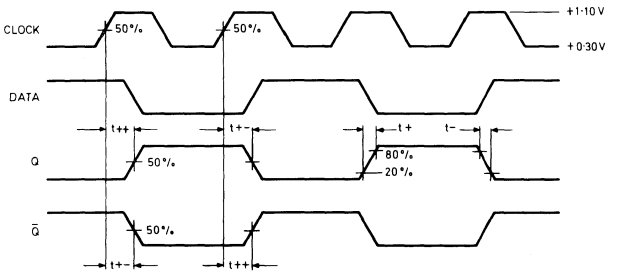


Fig. 4 Clock delay waveforms at +25°C

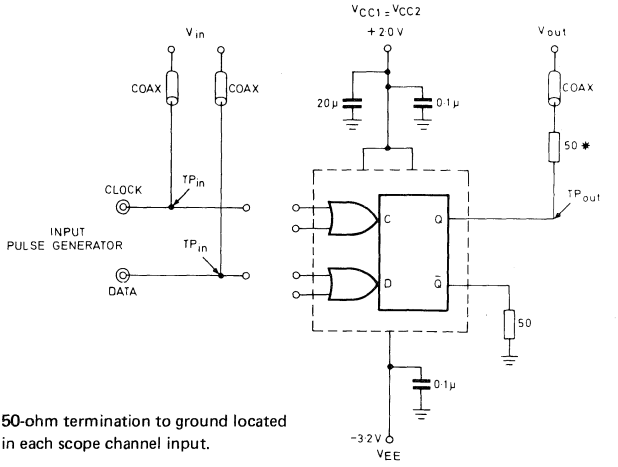
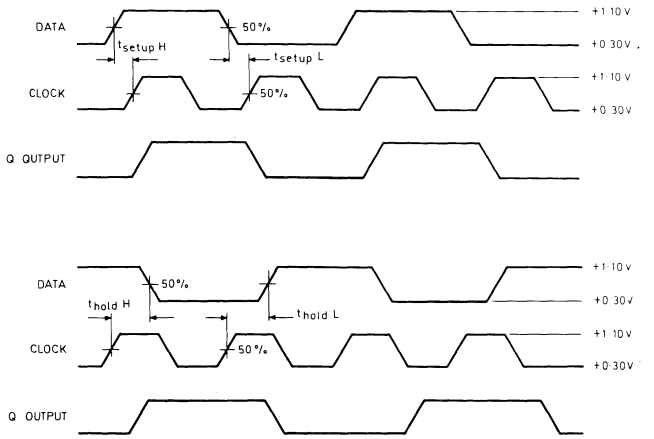


Fig. 5 Set up and hold time test circuit



Setup time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the date (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

Fig. 6 Set up and hold time waveforms

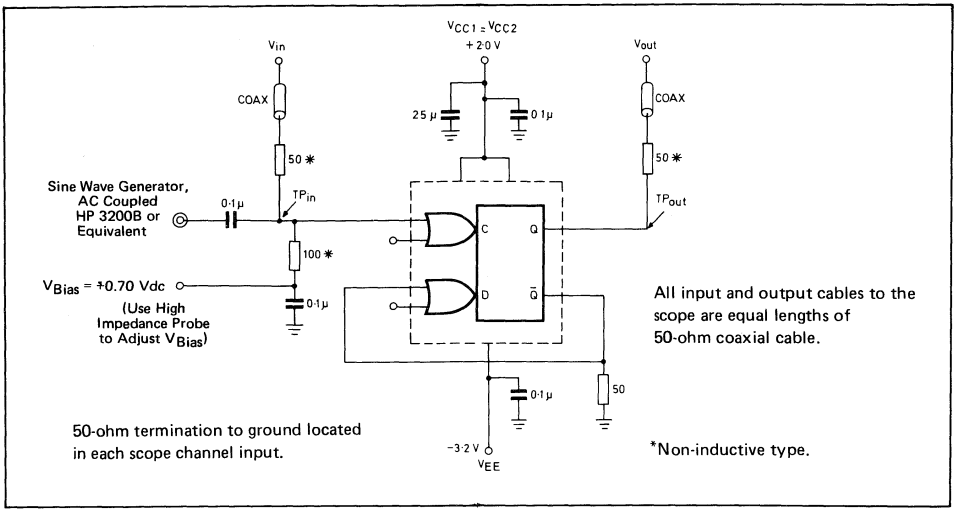
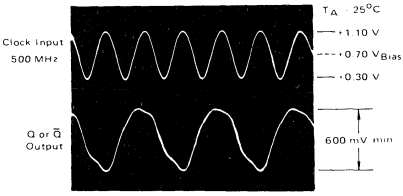


Fig. 7 Toggle frequency test circuit



The maximum toggle frequency of the SP1690 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts,

   OR

2. The device ceases to toggle (divide by two).

Fig. 8 Toggle frequency wavetorms

PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1692B
QUAD LINE RECEIVER

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.

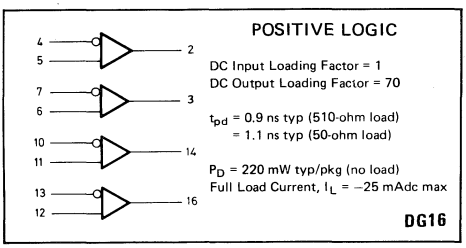


Fig. 1 Logic diagram of SP1692

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	From Pin 9	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485		−5.2
+75°C	−0.720	−1.830	−1.035	−1.035		−5.2

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	−1.35	−1.25	−1.30	−1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	1.0	1.5	1.0	1.5	1.1	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	1.1	1.7	1.1	1.7	1.2	1.9								
Rise Time	t_{2+}	2	1.4	2.1	1.4	2.1	1.5	2.3								
Fall Time	t_{2-}	2	1.2	2.1	1.2	2.1	1.3	2.3								

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8600A&B&M
250MHz ÷ 4 COUNTER

The SP8600 is a fixed ratio emitter coupled logic ÷4 counter with a specified input frequency range of 15—250 MHz. The operating temperature range is specified by the device code suffix letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C operation, 'M' denotes −40°C to +85°C.

Intended for use with an external bias arrangement and capacitive coupling to the signal source, the SP8600 can be either single driven, or double driven with two complementary input signals.

The outputs are complementary free collectors that can have their load resistors taken to any bias voltage up to 1.2V more positive than V_{EE}.

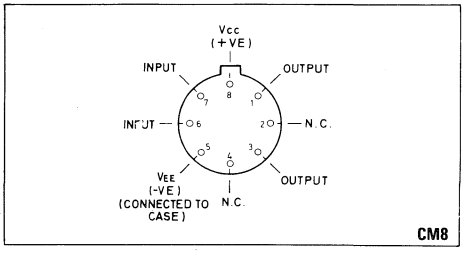


Fig. 1 Pin connections (bottom view)

FEATURES

- Low Power
- Free Collector Outputs to Interface to TTL
- 250 MHz ÷ 4 Over Full Military Temp. Range

APPLICATIONS

- Synthesizers — Mobile and Fixed
- Counters
- Timers

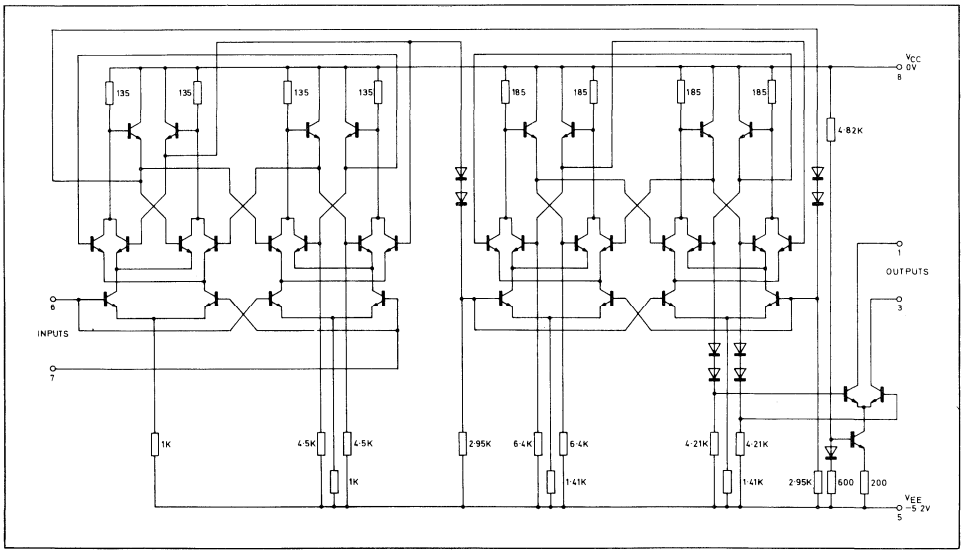


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade —55°C to +125°C
'B' grade 0°C to +70°C
'M' grade —40°C to +85°C

Supply voltage V_{CC} 400 to 800 mV p-p
V_{EE} 250 to 800 mV p-p
Input voltage (single driven — other input decoupled to ground plane)
Input voltage (double complementary input drive)
Input bias voltage — Bias chain as in test circuit (see Fig. 3 and operating notes).

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. input frequency	250	390*		MHz	Typical figure quoted at +25°C.
Min. input frequency with sinusoidal input			25	MHz	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	1.6			mA	Input f=250 MHz.
Power supply drain current		16*	25	mA	V_{EE} = —5.2V, V_{BIAS} as Fig. 3.

*At +25°C

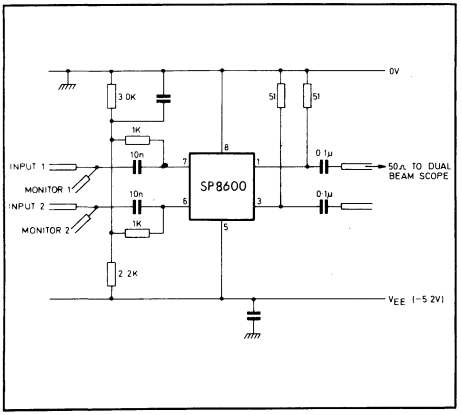


Fig. 3 Test circuit

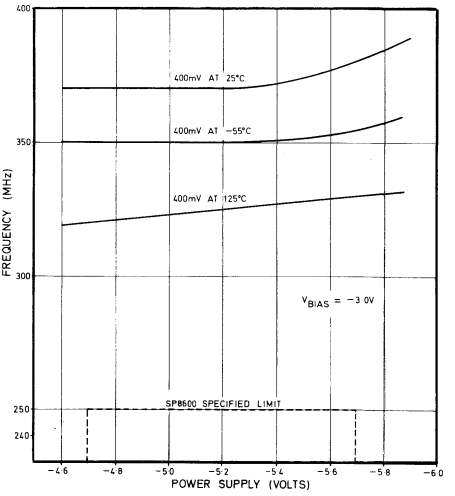


Fig. 4 Maximum input frequency v. power supply voltage (typical)

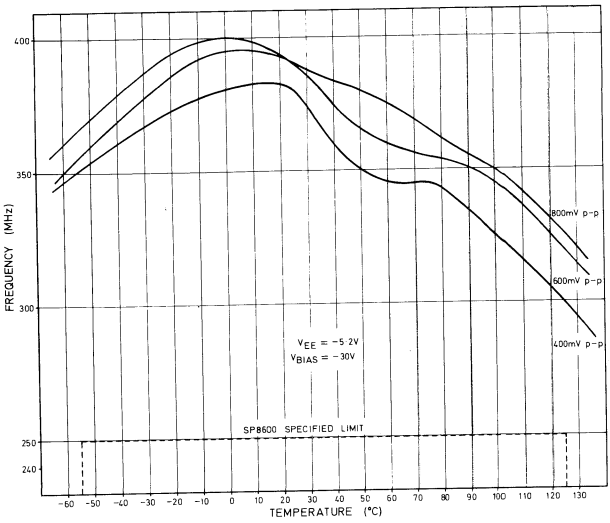


Fig. 5 Maximum input frequency v. temperature

OPERATING NOTES

The circuit performance obtained from the SP8600 is optimized if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias chain to set the DC potential on the inputs (see Fig. 3). No appreciable change in performance is observed over a range of DC bias from −2.5V to −3.5V.

Any tendency for the circuit to self-oscillate in the absence of input signal (or when the input signal is very small) can be overcome by offsetting the two inputs by approximately 40mV, using, for example, the bias arrangement shown in Fig. 6. The input wave form may be sinusoidal, but below 25 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate greater than 20V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with at least 2mA available from them. For satisfactory high frequency interfacing to ECL or Schottky TTL the circuit techniques illustrated in Fig. 7 are recommended.

For maximum frequency operation, it is essential that the output load risistor values be such that the output transistors do not saturate. If the load resistors are connected to the 0V rail, then saturation can occur with resistance values greater than 600Ω. Of course, if the load resistors are taken to a more positive potential, then higher values can be used. N.B. If only one output is used, the other output should be connected to 0V.

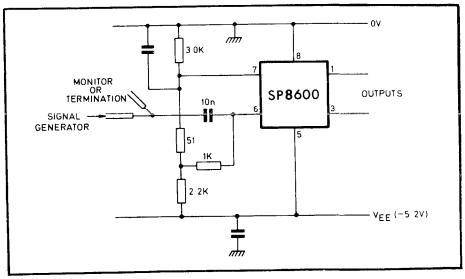


Fig. 6 Bias arrangement to prevent self-oscillation under no-signal conditions

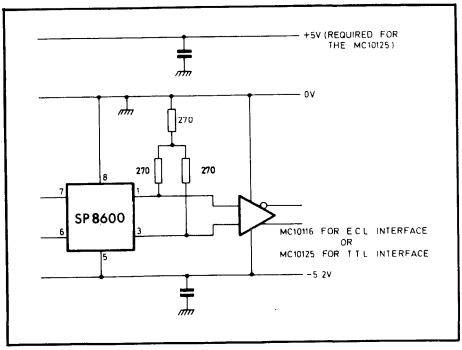


Fig. 7 ECL qnd Schottky TTL interfacing

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC}—V_{EE}	10V
Input voltage V_{IN}	Not greater than supply voltage in use
Bias voltage on o/p's V_{OUT}—V_{EE}	14V
Operating junction temperature	+175°C max.
Storage temperature	—55°C to +175°C

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8601A, B & M 150MHz ÷4

The SP8601 is a fixed ratio emitter coupled logic ÷4 counter with a maximum specified input frequency of 150 MHz but with a typical maximum operating frequency well in excess of this (see Typical Operating Characteristics). The operating temperature range is specified by the final coding letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C, and 'M' denotes −40°C to +85°C.

The SP8601 can be operated with single input drive or with double, complementary, I/P drive. It can be driven with direct coupling from ECL II levels (or from an SP8602 device), or it can be capacitively coupled to the signal source if an external bias is provided.

There are complementary free collector outputs that can have their external load resistor connected to any bias up to 12 volts more positive than V_{EE}.

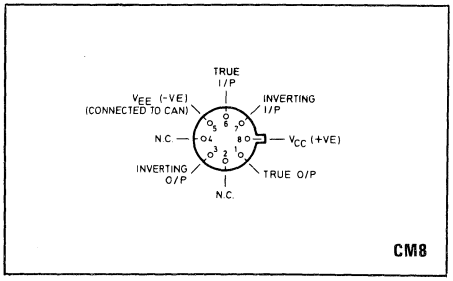


Fig. 1 Pin connections (bottom view)

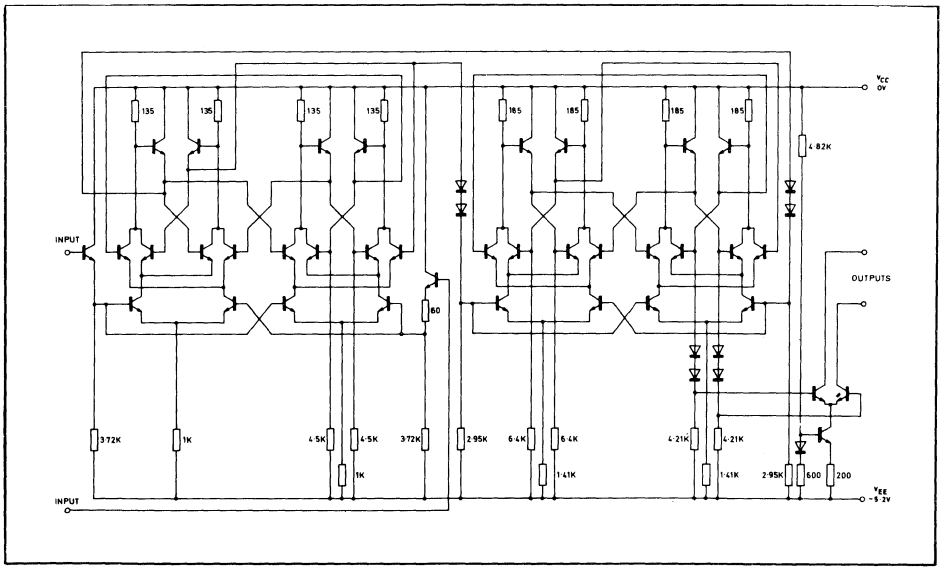


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade	−55°C to +125°C
'B' grade	0°C to +70°C
'M' grade	−40°C to +85°C
Operating supply voltage V_{CC}	0V.
V_{EE}	−5.2V ±0.25V
Input voltage (single drive — other input decoupled to ground plane)	400 to 800 mV (p-p)
Input voltage (double drive)	250 to 800 mV (p-p)
Bias voltage	Bias chain as in test circuit (see Fig. 2).

Characteristic	Value			Units	Conditions
	Min	Typ.	Max.		
Max. input frequency	150			MHz.	
Min. input freq. with sinusoidal input.			15	MHz.	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	1.6			mA	Input freq.= 150 MHz. R_{load} = 50Ω
Power supply drain current		18	25	mA	V_{EE} = −5.2V

OPERATING NOTES

Circuit performance obtained from the SP8601 is optimised if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally directly coupled into the device, which will tolerate a wide range of input bias voltages, but was designed for inputs from ECL II levels and can therefore be satisfactorily driven from SP8602 range of counters. The bias voltage on the input marginally affects the overall power consumption of the device (For typical operating characteristics with varying bias voltages see Fig. 4).

If it is not practicable to directly couple the input signal, then a bias chain similar to the one shown in Fig. 3 can be used.

The input waveform may be sinusoidal, but below about 10 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate of greater than 20 V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with 2 mA min. available from them. The output voltage swing obviously depends on the value of load resistor used and also the frequency of operation. The following table gives some typical examples of output voltage for different load resistors. With careful board layout to minimise capacitance these figures can easily be exceeded.

Min. Output Voltage	Load Resistor	Input Frequency
1.1V	1kΩ	120 MHz
320mV	200Ω	150 MHz
80mV	50Ω	180 MHz

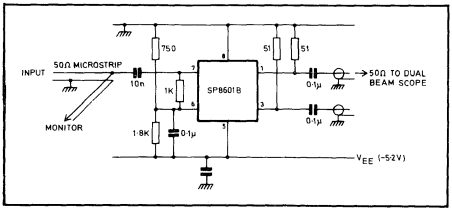
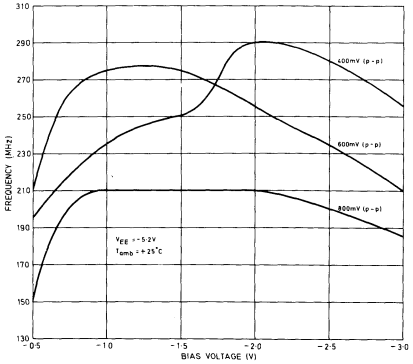


Fig. 3 Test circuit

TYPICAL OPERATING CHARACTERISTICS



NOTE: The value of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig. 4 Maximum input frequency v. bias voltage at single input drive levels of 400, 600 and 800 mV (typical device)

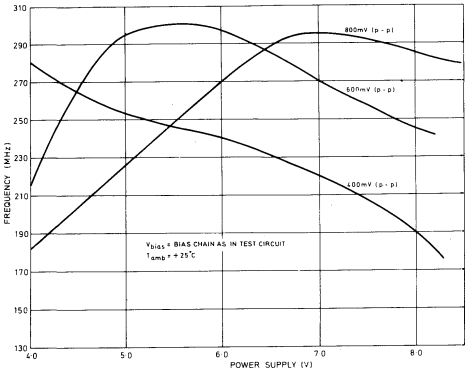


Fig. 5 Maximum frequency v. power supply voltage at single input drive levels of 400, 600 and 800 mV (typical device)

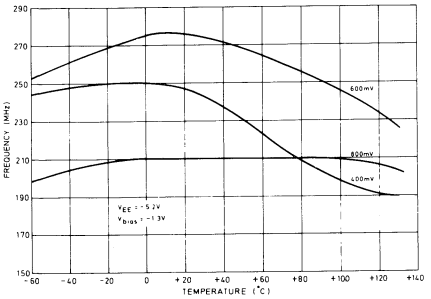


Fig. 6 Maximum input frequency v. temperature at single input drive levels of 400, 600 and 800 mV (typical device)

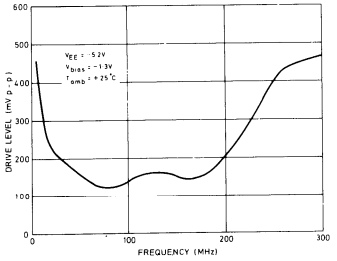


Fig. 7 Minimum single input drive level for correct operation v. input frequency (typical device)

APPLICATION NOTES

The SP8601 used with two SP8602 series ÷2 counters to give a 500 MHz divide-by-sixteen prescaler is shown in Fig. 8. Capacitors marked thus * may need to be increased in value for low frequency operation.

For correct operation when interfacing with TTL and ECL II the circuits shown in Figs. 9, 10 and 11 are recommended.

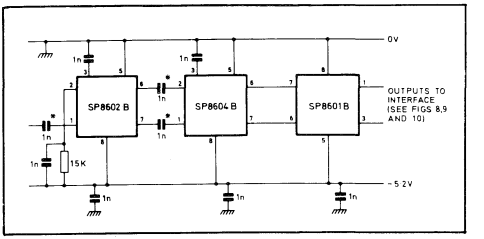


Fig. 8 Divide-by-sixteen prescaler

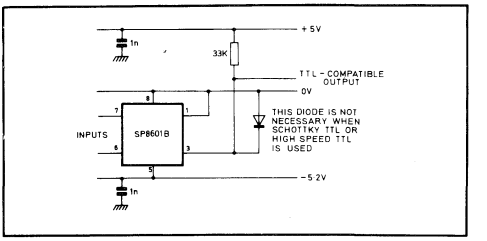


Fig. 9 TTL interface (fanout = 1 TTL gate)

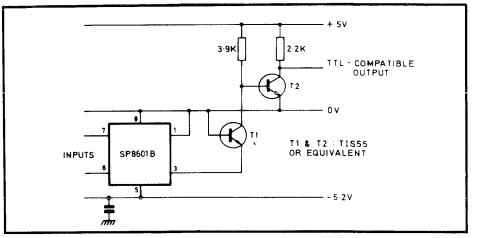


Fig. 10 High fanout TTL interface

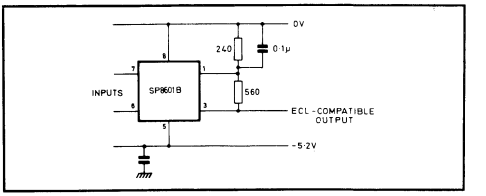


Fig. 11 ECL II interface

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	
V_{CC}—V_{EE}	10 V
Input voltage V_{in}	Not greater than the supply voltage in use
Bias voltage on outputs	
V_{out}—V_{EE}	14 V
(see Operating Notes)	
Operating junction temperature	+175°C
Storage temperature	−55°C to +175°C

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8602 A, B&M 500MHz÷2
SP8603 A, B&M 400MHz÷2
SP8604 A, B&M 300MHz÷2

The SP8602, SP8603 and SP8604 are fixed ratio ECL – 2 counters with maximum specified I/P frequencies of 500, 400 and 300 MHz respectively. The operating temperature range is specified by the final coding letter: 'A' denotes –55°C to +125°C, 'B' denotes 0°C to +70°C and 'M' denotes –40°C to +85°C.

The devices can be operated with single input drive or with double, complementary, input drive; in both cases the input is normally capacitively coupled to the signal source. Two complementary emitter follower outputs are provided.

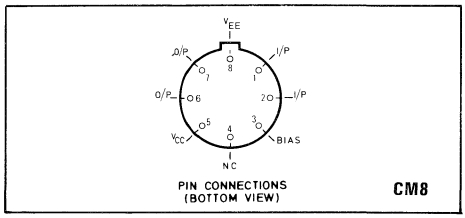


Fig. 1 Pin connections

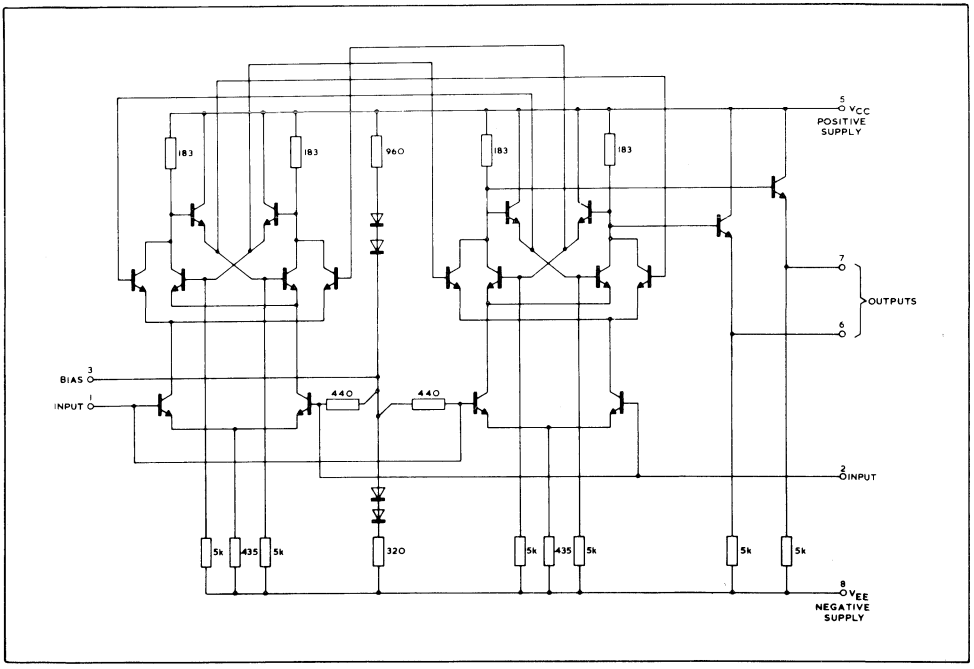


Fig. 2 Circuit diagram (all resistor values are nominal)

ELECTRICAL CHARACTERISTICS

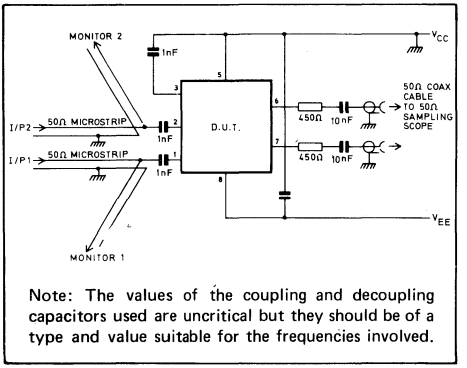
Test conditions (unless otherwise stated)

T_{amb} 'A' Grade	−55°C to +125°C
'B' Grade	0°C to +70°C
'M' Grade	−40°C to +85°C
Operating supply voltage: V_{cc}	0V
V_{ee}	−5.2V± 0.25V
Input voltage (single drive- other input and bias decoupled to ground plane)	400 to 800 mV p-p
Input voltage (double drive- bias decoupled to ground plane)	250 to 800 mV p-p
Output load	500Ω and 3pF

Characteristic	Type	Value				Conditions
		Min.	Typ.	Max.	Units	
Max. input freq.	SP8602A,B.M	500			MHz	V_{ee} = −5.2V
	SP8603A,B,M	400			MHz	V_{ee} = −5.2V
	SP8604A,B,M	300			MHz	V_{ee} = −5.2V
Min. input freq. with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave input for correct operation	All		30	100	V/μS	single input drive
Output voltage swing	All	400			mV	V_{ee} = −5.2V T_{amb} = −55°C to +70°C
Output voltage swing	SP602A	350			mV	V_{ee} = −5.2V T_{amb} = +125°C I/P freq. = 500 MHz
Power supply drain current	All		12	20	mA	V_{ee} = −5.2V See note 1

NOTES

1. In practice, the 3.5kΩ resistors specified in the test circuit (Fig.3) are not essential; omission of these resistors will reduce the maximum supply current to 18mA.



Note: The values of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig. 3 Test circuit

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{cc} - V_{ee}$	8V
Input voltage V_{in}	Not greater than the supply voltage in use
Output current I_{out}	10 mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the output emitter-followers are inadvertently shorted to ground. All components used in the circuit layout should be suitable for the frequencies involved, and outside a controlled impedance environment, leads and connections should be kept short to minimise stray inductance.

The signal source is normally capacitively coupled to the input. A 1000pF capacitor is usually sufficient. If the input signal is likely to be interrupted a 15KΩ resistor should be connected between the input and the negative rail. In the single drive case it is preferable to connect the resistor to the input not in use – in the double drive case either input can be used. The addition of the input pulldown resistor causes a slight loss of input sensitivity, but it prevents circuit oscillation under no-signal conditions.

The input waveform may be sinusoidal, but below about 40 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than the amplitude. A square wave input with a slew rate of more than 100 V/μS will permit correct operation down to DC.

The output voltage swing can be increased by the addition of a DC load to the output emitter followers. Pulldown resistors of 1.5 K to the negative rail provide an increase of typically 25% in the output voltage swing.

APPLICATION NOTES

SP8602B and SP8604B interfacing to E C L 10 000 and E C L III

By increasing the output voltage swing using external pulldown resistors (see operating notes), the SP8604B can be coupled directly into an E C L III or E C L 10 000 gate, but there is a reduction of the noise immunity. Where noise immunity is important the device can be connected to an E C L 10 000 or E C L III line receiver.

Divide-by-16 frequency scaler.

The SP8602B and SP8604B interfacing with the SP8601B and high-speed TTL to give a divide-by-16 frequency scaler is shown in Fig. 4.

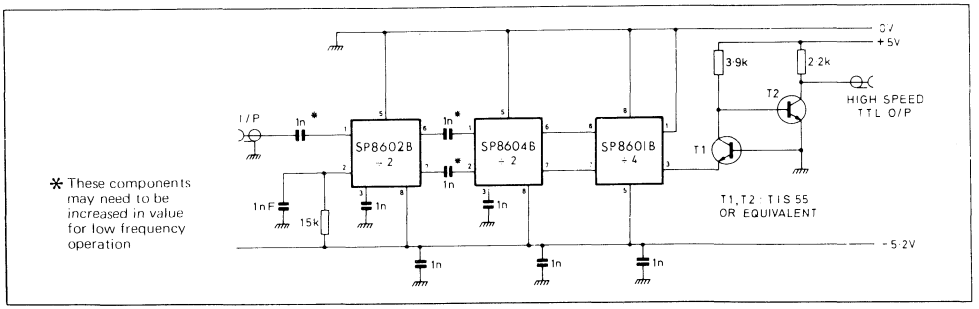


Fig. 4 Divide-by-16 frequency scaler

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH-SPEED DIVIDERS

SP8607 A, B&M
600 MHz ÷ 2

The SP8607 is a divide-by-2 counter with a minimum guaranteed toggle frequency of 600 MHz over a 0°C to +70°C temperature range. The device is designed for capacitive coupling to the signal source to either of the two inputs and it has two complementary emitter follower outputs. Power dissipation is typically only 70mW with a 5.2V supply.

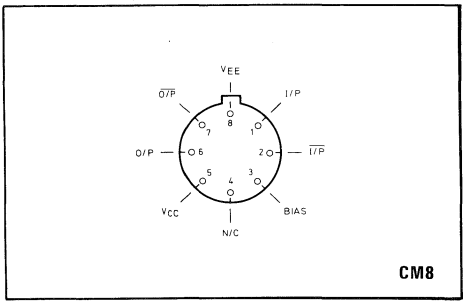


Fig.. 1 Pin connections

FEATURES

- 600 MHz Operation
- −55°C to 125°C Guaranteed for 'A' grade
- Only 70mW Dissipation at 5.2V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Connections as test circuit, Fig. 3
T_{amb}: (A grade) −55°C to +125°C
(B grade) 0°C to +70°C
(M grade) −40°C to +85°C
Supply voltage V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V
Specified input voltage range: 400 to 800mV p-p

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage $\|V_{CC} - V_{EE}$	8V
Input Voltage DC	⩽ Supply
Input Voltage AC	2.5V p−p
Output Current	15mA
Operating Junction Temp.	+150°C
Storage Temp Range	−55°C to + 150°C

Characteristic	Value			Units	Conditions
	Min	Typ.	Max		
Max. toggle frequency	600	800		MHz	
Min. input frequency (sine wave)		50		MHz	
Min. slew rate of square wave input for correct operations to OHz		40	100	V/μs	
Output voltage swing	400			mVp-p	V_{EE} = −5.2V, f_{in} = 600 MHz
Output voltage levels					
V_{OH}		−0.75		V	f_{in} = OHz
V_{OL}		−1.5		V	
Input impedance		400		Ω	f_{in} = OHz
O/P pulldown resistors		4.0		kΩ	
Bias voltage level		−2.6		V	2.7kΩ resistor from pin 3 to V_{CC}
Power supply drain current		14	18	V	V_{EE} = −5·2V

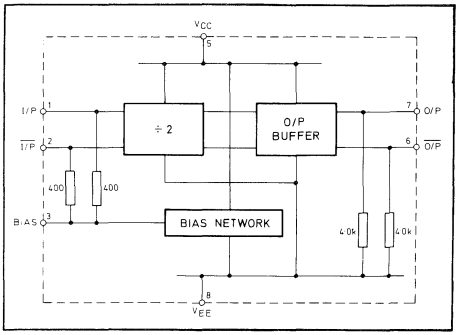


Fig. 2 SP8607 block diagram

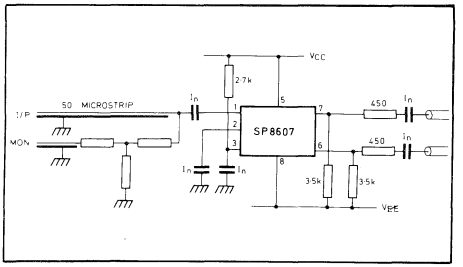


Fig. 3 Test circuit for SP8607

OPERATING NOTES

All components used with the SP8607 should be suitable for the frequencies involved, resistors and capacitors should be of low inductance types and unterminated loads should be kept short to minimise uncounted reflections. The test circuit uses positive earth because this minimises noise problems and the danger of accidently shorting the O/P transistors to a negative voltage. However, the device will operate satisfactorily and to the specification, with a negative earth provided that the positive supply is well decoupled to the UHF earth.

There are two complementary inputs connected to an internally-generated temperature-compensated bias point via two 400 ohm resistors. The signal source would normally be capacitively coupled to one of the inputs and the other should be decoupled to earth. If two complementary input signals are available (when cascading SP8607s for example) both inputs should be used

The input signal can be directly connected to the device either by using a voltage dropping network or by using split power supplies (see Fig. 4). In this mode the device is very tolerant of the actual values of V_{CC} and V_{EE} although $V_{CC} - V_{EE}$ should stay within 5.2V ± 0.25V. A 2.7kΩ resistor is connected from V_{CC} to the bias pin in the test circuit because this greatly improves the device's ability to operate with large input signals

It is important that pins 2 and 3 are decoupled by a capacitor in the range 100 – 1000pF because device sensitivity can be reduced by decoupling to a poor earth

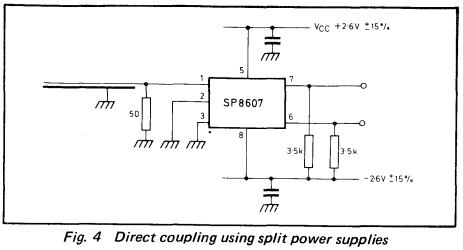


Fig. 4 Direct coupling using split power supplies

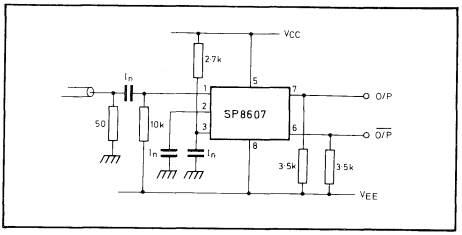


Fig. 5 SP8607 with input pulldown resistor

In the absence of an input signal, or if the input signal is of very low amplitude, the device may give an output signal of about 250 MHz. This is due to the balanced nature of the internal ÷ 2 circuit and can be stopped if required by connecting a 10 kohm resistor between the input and the negative rail. (See Fig. 5). This causes a drop in sensitivity of about 100 mV but typical devices still easily meet the 400 – 800 mV input amplitude specification. With sine wave inputs below 50MHz the SP8607 miscounts because the slew rate of the input signal is too slow. Below this frequency a square wave input is needed with a slew rate of 100V/μ or more.

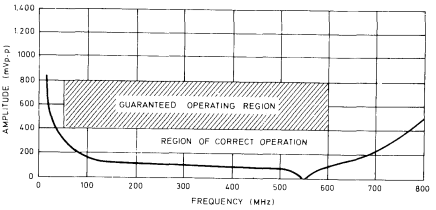


Fig. 6 Typical operating characteristic

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8616B&M 1 GHz ÷4 SP8615B&M 900MHz÷4
SP8614B&M 800MHz÷4 SP8613B&M 700MHz÷4

The SP8616 series of UHF counters are fixed ratio ÷ 4 asynchronous emitter coupled logic counters with, in the case of the SP8616B, a maximum operating frequency in excess of 1GHz, over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100Ω lines and interfacing to ECL with the same positive supply. The SP8616 series require supplies of 0V and −7.4V (± 0.4V).

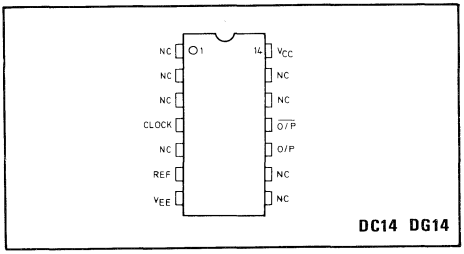


Fig. 1 Pin connections

FEATURES

- DC to 1GHz operation.
- 0°C to 70°C operation guaranteed at maximum specified frequency and over a wide dynamic input range.
- Complementary emitter follower O/Ps, ECL compatible.

APPLICATIONS

- UHF Instrumentation, Including Counters and Timers
- Prescaling for UHF Synthesisers.

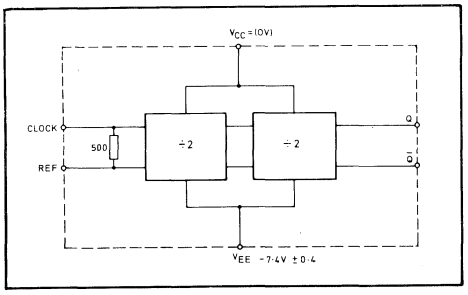


Fig. 2 Functional diagram

QUICK REFERENCE DATA

- V_{CC} = 0V
- V_{EE} = −7.4V ± 0.4V
- Input Voltage Range 400mV to 1.2V (see Fig. 3)
- Output Voltage Swing 700mV Typ.
- Temp. Range: 'B' Grade 0°C to +75°C
  'M' Grade −40°C to + 85°C

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$	10 volts
Input voltage	V_{IN} ac	2.5 volts p-p
Output current		15mA
Storage temperature range		−55°C to +150°C
Maximum operating function temperature		+150°C

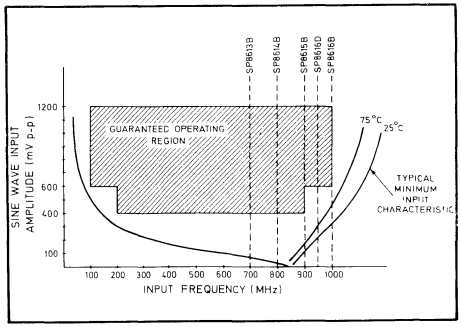


Fig. 3 Specified range of operation

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated).

T_{amb} = 'B' grade: 0°C to +70°C; 'M' grade: −40°C to +85°C
Supply voltage
V_{CC} = 0V
V_{EE} = −7.4V ± 0.4V

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.toggle frequency	SP8616	1000			MHz	V_{IN} = 600mV to 1.2Vp-p (see Fig. 3)
	SP8615	900			MHz	V_{IN} = 400MHz to 1.2V p-p
	SP8614	800			MHz	V_{IN} = 400MHz to 1.2V p-p
	SP8613	700			MHz	V_{IN} = 400MHz to 1.2V p-p
Min.toggle frequency for correct operation with sine wave input	ALL			200	MHz	V_{IN} = 400mV to 1.2V p-p
Min.toggle frequency for correct operation with sine wave input	ALL			100	MHz	V_{IN} = 600mV to 1.2V p-p
Min slew rate for square wave input to guarantee operation to 0Hz	ALL			200	V/μs	
Output voltage swing	ALL	500	700		mV	
Power supply drain current	ALL		45	60	mA	V_{EE} = −7.4V

Toggle Frequency Test Board Layout

1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

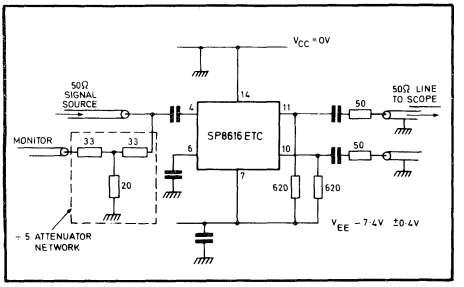


Fig. 4 Toggle frequency test circuit

OPERATING AND APPLICATION NOTE

The SP8616 series of dividers are very simple to use but normal high frequency rules should be followed for optimum performance, for example, all connections should be kept short, the capacitors and resistors should be types suitable for the frequencies involved, etc.

The input is normally capacitively coupled to the signal source. There is an internal 500Ω resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane.

The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 5).

$V_{CC} - V_{EE}$ should be kept inside the specified 7.4 volts ± 0.4 volts but the actual value of V_{CC} relative to earth is not very critical and can be varied between 4.0V and 6.0V with only a small effect on performance. A V_{CC} of about 5.2V is the optimum for full temperature range operation.

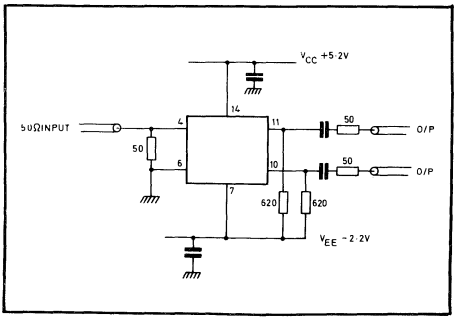


Fig. 5 Circuit for using the input signal about earth potential

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self oscillate with an output frequency of approximately 200MHz. This can be prevented by connecting a 10kΩ resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8616 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL II directly and to ECL III using two resistors. (See Fig. 6).

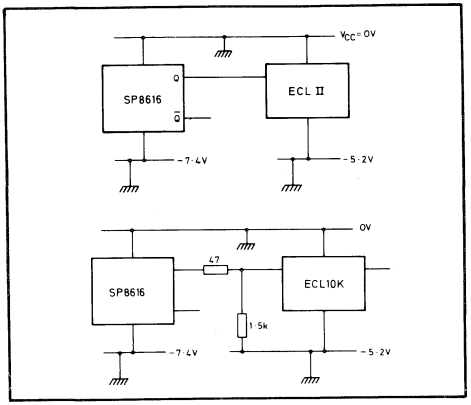


Fig. 6 Interfacing SP8616 series to ECL II and ECL III

The input impedance of the SP8616 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum input signal requirement. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

A commercially available hybrid amplifier can be used to drive the SP8616 (see Fig. 7).

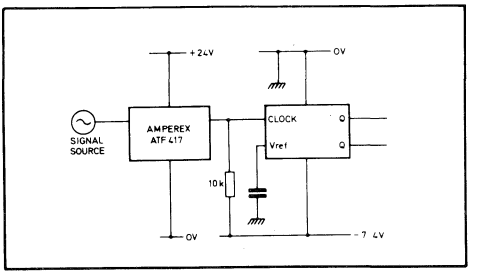


Fig. 7 The SP8616 driven by a commercially available hybrid amplifier. The Amperex ATF417 output is internally capacitively coupled.

Note: The Amperex ATF 417 output is internally capacitively coupled.

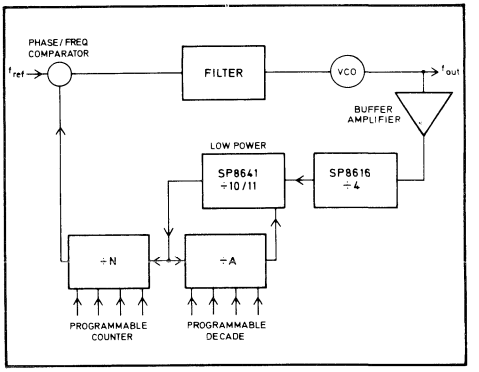


Fig. 8 A 1GHz synthesiser loop

The SP8616 series can be used in instrumentation for direct counting applications up to 1GHz and in frequency synthesisers.

In a frequency synthesiser, the SP8616 and the SP8641 can be used together (see Fig. 8).

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8619B 1.5GHz ÷ 4
SP8617B 1.3GHz ÷ 4

The SP8619 series of UHF counters are fixed ratio ÷4 asynchronous emitter coupled logic counters with, in the case of the SP8619B a maximum operating frequency in excess of 1.5GHz over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100 ohm lines and interfacing to ECL with the same positive supply. The SP8619 series require supplies of 0V and −6.8V (± 0.35V).

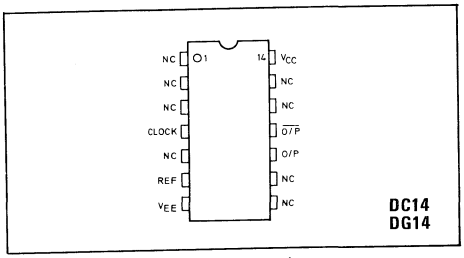


Fig. 1 Pin connections

FEATURES

- DC to 1.5GHz Operation
- 0°C to 70°C Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range
- Complementary Emitter Follower O/Ps, ECL10K and ECL III Compatible

APPLICATIONS

- UHF Instrumentation, Including Counters and Timers
- Prescaling for UHF Synthesisers

QUICK REFERENCE DATA

- $V_{CC} = 0V$ $V_{EE} = -6.8V \pm 0.35V$
- Input Voltage Range 400mV to 1.2V p-p
- Temperature Range 0°C to +70°C
- Output Voltage Swing 800mV Typ.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $|V_{CC} - V_{EE}|$ 10V
Input voltage V_{INac} 2.5V p-p
Output current 15mA
Storage temperature range −55°C to +150°C
Maximum operating function temperature +150°C

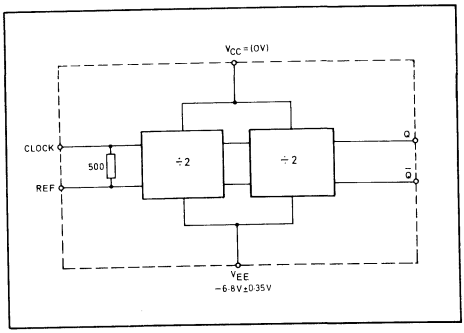


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
$T_{amb} = 0°C$ to $+70°C$
Supply voltage $V_{CC} = 0V$ $V_{EE} = -6.8 \pm 0.35V$
Input voltage 400 – 1200mV p-p

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. toggle frequency	SP8619B	1.5			GHz	
	SP8617B	1.3			GHz	
Min. toggle frequency for correct operation with sine wave input	All			150	MHz	V_{IN} = 600mV to 1.2Vp-p
Min. toggle frequency for correct operation with sine wave input	All			100	MHz	V_{IN} = 800mV to 1.2Vp-p
Min slew rate for square wave input to guarantee operation to 0Hz	All			200	V/µs	
Output voltage swing	All	600	800		mV	
Power supply drain current	All		80	110	mA	$V_{EE} = -7.15V$

Toggle Frequency Test Board Layout

1. All connections to the device are kept short
2. The capacitors are leadless ceramic types
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

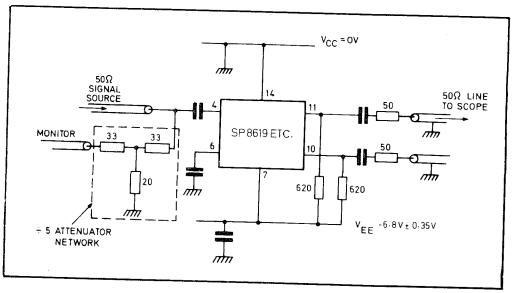


Fig. 3 Toggle frequency test circuit

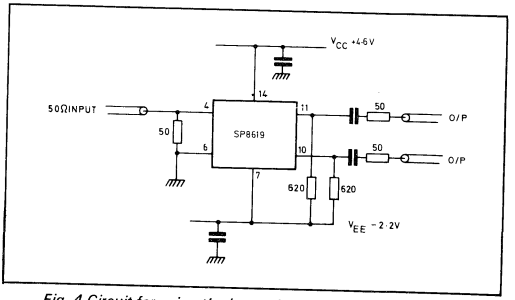


Fig. 4 Circuit for using the input signal about earth potential

OPERATING AND APPLICATION NOTE

The SP8619 series of dividers are very simple to use but normal high frequency rules should be followed for optimum performance - for example, all connections should be kept short and the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane.

The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 4).

$|V_{CC} - V_{EE}|$ should be kept inside the specified 6.8V $\pm$0.35V but the actual value of V_{CC} relative to earth is not very critical and can be varied between 4.2V and 5.0V with only a small effect on performance. A V_{CC} of about 4.6V is the optimum for full temperature range operation.

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self-oscillate with an output frequency of approximately 300MHz. This can be prevented by connecting a 10k ohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8619 will miscount with low frequency sine-wave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (see Fig. 5).

The input impedance of the SP8619 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum input signal requirement. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8619 series can be used in instrumentation for direct counting applications up to 1.5GHz and in frequency synthesisers.

In a frequency synthesiser, the SP8619 and the SP8643 can be used together (see Fig. 6).

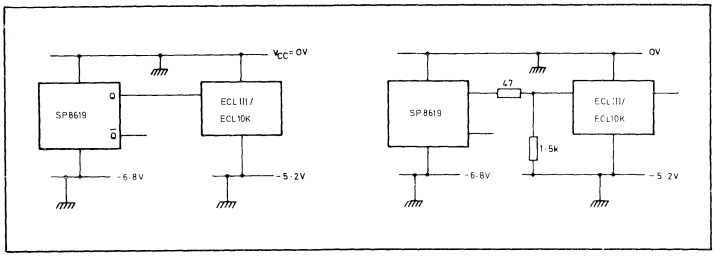


Fig. 5 Interfacing SP8619 series to ECL 10K and ECL III

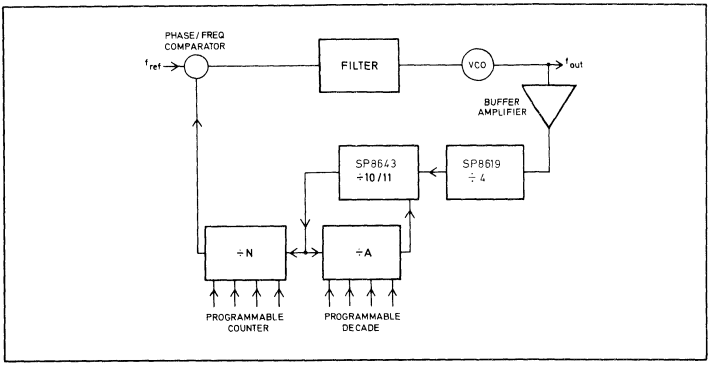


Fig. 6 A 1.5GHz synthesiser loop

PLESSEY
SEMICONDUCTORS

SP8000 SERIES

HIGH SPEED DIVIDERS

÷5 COUNTERS

SP8620 A,B & M (400MHz)
SP8621 A,B & M (300MHz)
SP8622 A,B & M (200MHz)

The SP8620, SP8621 and SP8622 are fixed ratio emitter-coupled logic ÷5 counters with specified input frequency ranges of DC to 400MHz (SP8620), 300MHz (SP8621) and 200MHz (SP8622) respectively. The operating temperature is specified by the final coding letter: −55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade) and −40°C to +85°C ('M' grade).

The counter is normally capacitively coupled to the signal source and is specified with an input signal range of 400−800mv p-p (−4dBm to +22dBm). There are two bias points on the circuit that should be capacitively decoupled to the ground plane.

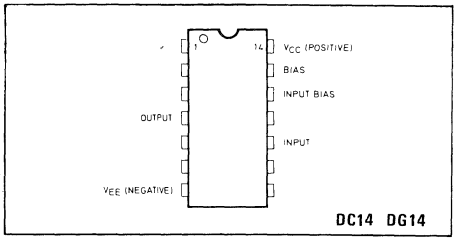


Fig.1 Pin connections (bottom view)

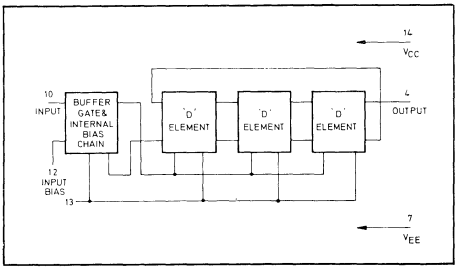


Fig.2 Circuit diagram (all resistor values are nominal)

FEATURES

- D.C. to 400MHz Operation.
- Temperature Ranges of −55°C to +125°C ('A' Grade), 0°C to +70°C ('B' Grade) and −40°C to +85°C ('M' Grade) Over Full Specified Input Range and Frequency.

APPLICATIONS

- Frequency Counters and Timers
- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Tamb: 'A' grade: −55°C to +85°C
'B' grade: 0°C to +70°C
'M' grade: −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{IN}	Not greater than supply
Output current I_{OUT}	15mA
Operating junction temperature	+150°C
Storage temperature	−55° to +150°C

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. input frequency	SP8620	400			MHz	
	SP8621	300			MHz	
	SP8622	200			MHz	
Min. input frequency with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave input for correct operation	All		30	100	V/μS	
Output voltage swing	All	400	800		mV	V_{EE} = −5.2V
Power supply drain current	All		55		mA	V_{EE} = −5.2V

OPERATING NOTES

It is recommended that a positive earth plane is used for the circuit layout, thus preventing damage if the output is short-circuited to earth.

The signal source is normally capacitively coupled to the input (see Fig. 3). A 1000pF capacitor is suitable at high frequencies, but if lower frequency operation is also required, say below 10MHz, then an additional capacitor should be connected in parallel. The device can be DC coupled if it is required – see Fig. 4.

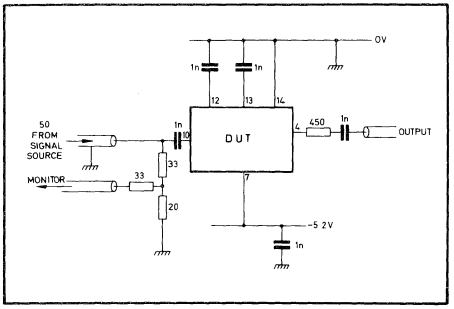


Fig.3 Test circuit

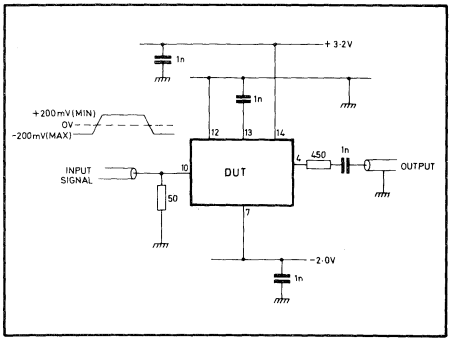


Fig.4 Divide by 16 frequency scaler

The circuit may self oscillate when there is no input signal or when the input signal is well below the specified input signal. This can be prevented by connecting a 15kΩ resistor between the input and the negative rail. This causes a loss in sensitivity of up to 100mV p-p.

The input waveform may be sinusoidal, but below about 20MHz the circuit tends to malfunction on minimum amplitude input signals and the condition becomes worse as the frequency is decreased. This is because correct operation of the circuit depends on the slew rate of the input signal. A square wave input with a slew rate greater than 100V/μS ensures correct operation down to DC.

The output swing of the devices can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5kΩ will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8620 devices to interface directly to ECL II devices with no loss in noise immunity. If the devices are required to interface to ECL III or ECL 10,000 then an interface similar to Fig. 5 should be used.

The values of the decoupling capacitors are not critical, but they should be of a type suitable for the frequencies involved.

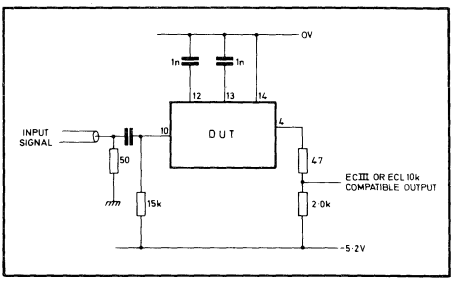


Fig. 5 Interfacing to ECL III or ECL 10,000

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8630 A, B&M
600MHz DECADE COUNTER
SP8631A, B&M
500MHz DECADE COUNTER
SP8632 A, B&M
400MHz DECADE COUNTER

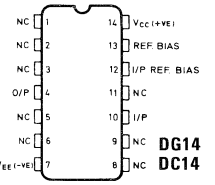
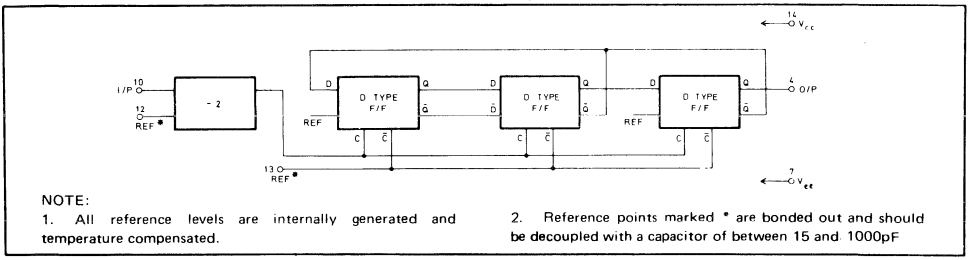


Fig. 1 Pin connections

GENERAL DESCRIPTION

The SP8630/1/2 counters are fixed ratio ÷ 10 circuits using emitter coupled logic, with maximum specified counting frequencies of 600, 500 and 400 MHz respectively, over temperature ranges of −55°C to +125°C, 0°C to 70°C and −40°C to +85°C. A 6:4 mark/space square wave is provided at the emitter follower output. The input is normally single driven and capacitively coupled to the signal source. There are two bias points on the circuit which should be capacitively coupled to the ground plane.



NOTE:
1. All reference levels are internally generated and temperature compensated.
2. Reference points marked * are bonded out and should be decoupled with a capacitor of between 15 and 1000pF

Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless stated otherwise):

Tamb: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'C' grade −40°C to +85°C

Operating supply voltage
V_{CC} 0V
V_{EE} −5.2V ± 0.25V
Input voltage 400 to 800 mV (p-p)
Output load 500Ω & 3pF.

NOTE: The maximum input frequency is guaranteed at V_{EE} = −5.2V. For typical operating characteristics with power supply variations see Fig.5, which shows that the maximum operating frequency of a typical device increases with increasing power supply voltage

Characteristic	Type	Value			Units	Conditions
		Min	Typ	Max		
Max input freq.	SP8630	600			MHz	
	SP8631	500			MHz	
	SP8632	400			MHz	
Min input freq. with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave I/P for correct operation	All		30	100	V/μs	
Output voltage swing	All	400	600		mV	V_{EE} = −5.2V
Power supply drain current			70		mA	V_{EE} = −5.2V

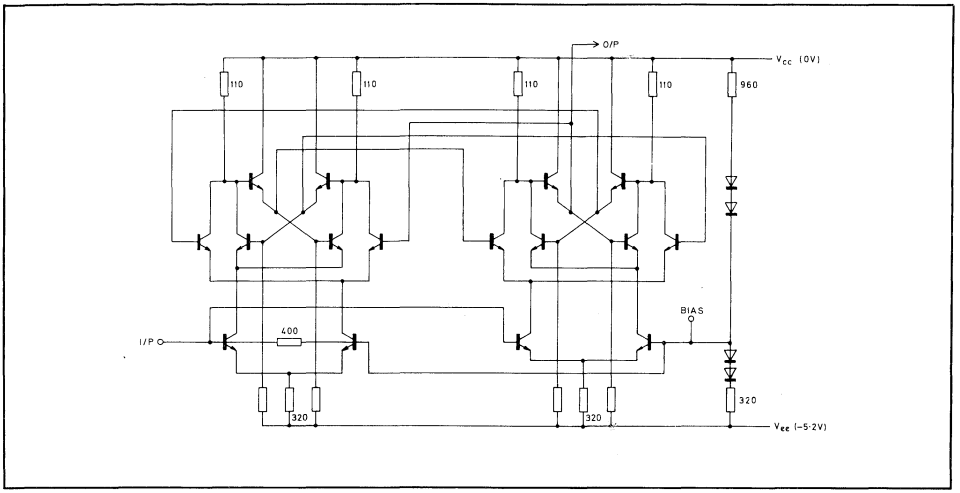


Fig. 3 Circuit diagram of 1st element (–2) showing input biasing arrangement

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the emitter follower outputs are inadvertantly shorted to ground.

The signal source is normally capacitively coupled to the input: 1000 pF is usually sufficient. If the input signal is likely to be interrupted a 15 k ohm resistor should be connected between the input pin and the negative rail to prevent circuit oscillation under no-signal conditions. The addition of the pulldown resistor causes a slight loss of sensitivity of the device, but this does not normally cause problems in practice.

The input waveform may be sinusoidal, but below 40 MHz the operation of the circuit becomes dependent on the slew rate of the waveform rather than the amplitude. A square wave input with a slew rate of 100 V/μs will allow correct operation down to DC. At high frequencies, increasing drive level above minimum typically increases the max. operating frequency by up to 25%

The output swing of the device can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5k ohms will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8630 series devices to drive directly into ECL II devices with no loss in noise immunity.

The value of capacitance needed for the decoupling capacitors is not critical. Values down to 15 pF have been found satisfactory in practice.

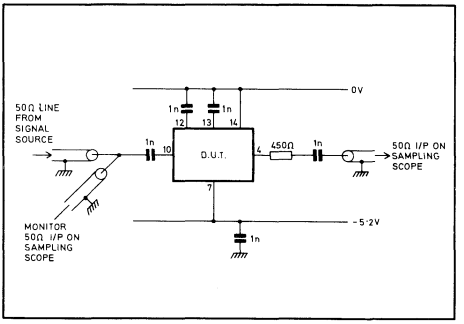


Fig. 4 Test circuit

Test Circuit Notes

The values of the coupling and decoupling capacitors are uncritical but they should be of a type and value suitable for the frequencies involved.

All connections should be physically short when not in a 50Ω environment to minimise reflections due to mismatching.

The +ve pin should be connected to a low impedance earth plane to minimise feed-through of the input signal to the output.

Typical Operating Characteristics

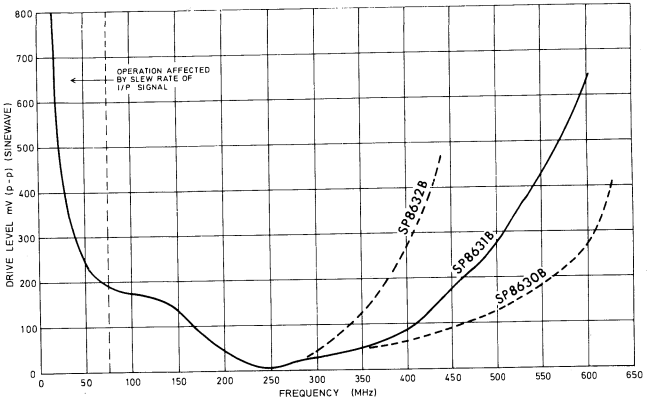


Fig. 5 Minimum drive level v. input frequency at +25 C

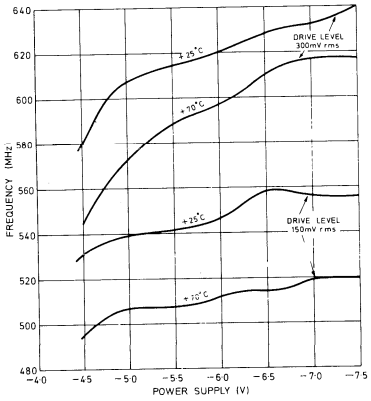


Fig. 6 Max. operating frequency v. power supply voltage for a typical SP8631B

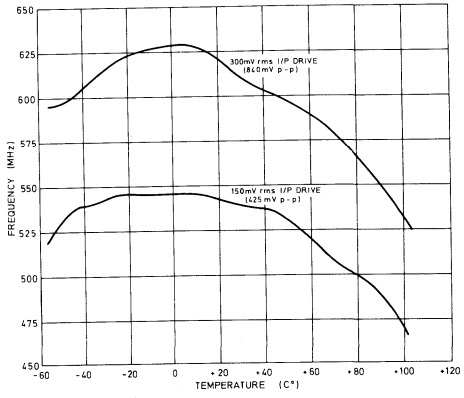


Fig. 7 Max. operating frequency v. ambient temperature for a typical SP8631B (Vcc = −5.2V)

APPLICATION NOTES

Direct coupling to the SP8630 series.

It can be seen from the circuit diagram that the input arrangement of the SP8630 series is not compatible with the normal ECL logic levels. The input reference level is approximately −3.2 volts but it is not well defined and has a temperature coefficient of approximately −1.6 mV/°C. If DC coupling is required, the input would have to be larger than would be the case with capacitive coupling.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	8V.
Input voltage V_{IN}	Not greater than the supply voltage in use
Output current I_{OUT}	15 mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8634B ÷ 10 700 MHz
SP8636B ÷ 10 500 MHz
SP8635B ÷ 10 600 MHz
SP8637B ÷ 10 400 MHz

The SP8634B, SP8635B, SP8636B and SP8637B are divide-by-ten circuits with binary coded decimal outputs for operation from DC up to specified input frequencies of 700, 600, 500 and 400 MHz, respectively, over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

FEATURES

- Direct gating capability at up to 700 MHz
- TTL- compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

APPLICATIONS

- Counters
- Timers
- Synthesisers

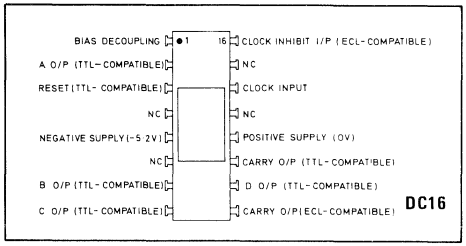


Fig. 1 Pin connections (top)

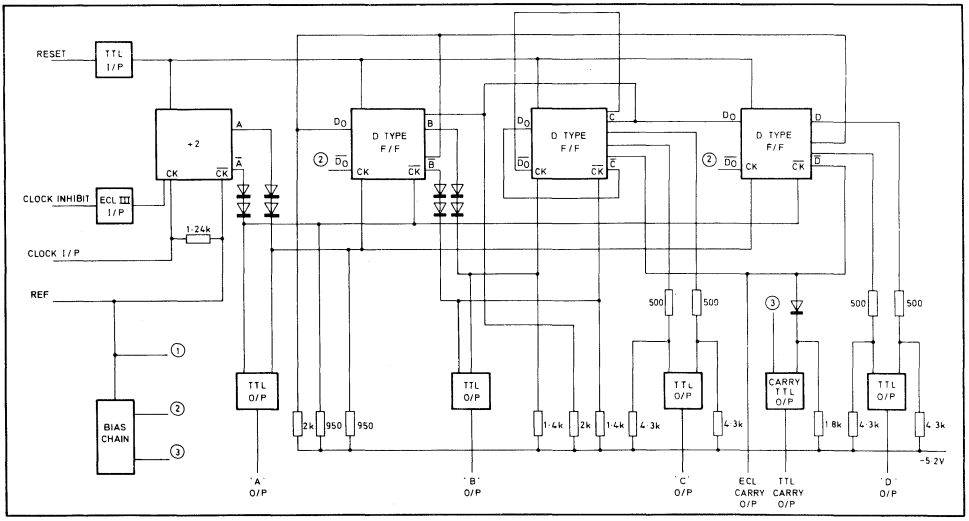


Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated)

T_{amb}		0°C to +70°C
Power Supplies	V_{CC}	0V
	V_{EE}	−5.2V ± 0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input (pin 14)					
Max. input frequency					
SP8634B	700			MHz	Input voltage 400-800mV p-p
SP8635B	600			MHz	
SP8636B	500			MHz	
SP8637B	400			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
Logic levels					
High (inhibit)	−0.960			V	T_{amb} = +25°C
Low			−1.650	V	(see Note 1)
Edge speed for correct operation at maximum clock I/P frequency			2.5	ns	10%–90%
Reset input (pin 3)					
Logic levels					
High (reset)	See Note 2				
Low			+0.4	V	
Reset ON time	100			ns	
TTL outputs ABCD (pins 2,7,8,10)					See Note 3 and Fig. 4
Output Voltage					
High	+2.4			V	10k Ω resistor and TTL gate from O/P
Low			+0.4	V	to +5V rail
TTL carry output (pin 11)					
Output Voltage					
High state	+2.4			V	5kΩ resistor and 3 TTL gates from o/p
Low			+0.4	V	to 5V rail
ECL carry output (pin 9)					
Output Voltage					
High	−0.975			V	T_{amb} = +25°C External current
Low			−1.375	V	= 0mA (See Note 4)
Power supply drain current		75	90	mA	V_{EE} = 5.2V

NOTES

1. The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8kΩ resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device.
3. These outputs are current sources which can be readily made TTL-compatible voltages by connecting them to +5V via 10kΩ resistors.
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

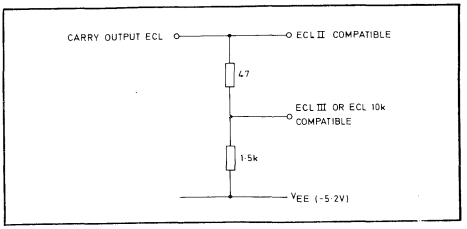


Fig. 3 ECL III/ECL 10000 interfacing

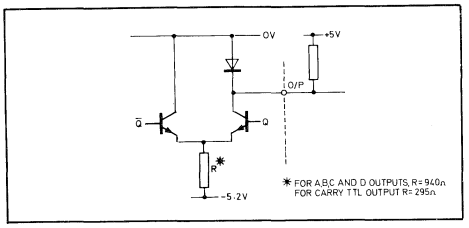


Fig. 4 TTL carry and ABCD output structure

OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system – the ECL and the decade counter being connected between voltage rails of OV and –5.2V and the TTL between voltage rails of OV and +5.0V. Provided that this is done ECL and TTL compatability is achieved (see Figs. 4 and 5).

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor – preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{CC} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

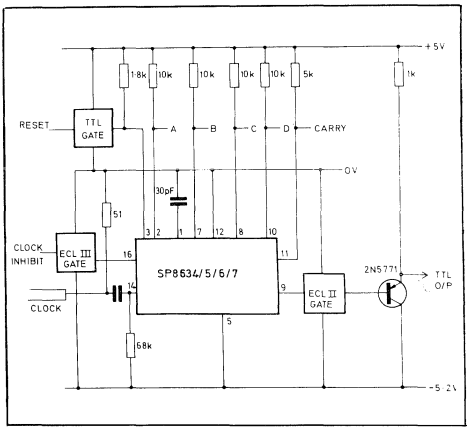


Fig. 5 Typical application configuration

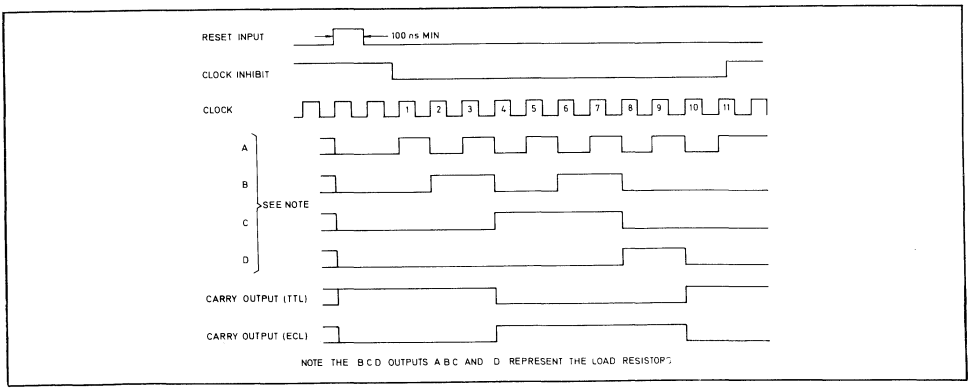


Fig. 6 Decade counter timing diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	8V
Clock inhibit voltage	Not greater than the supply voltage in use
Clock input voltage	2V pk/pk
Bias voltage (V_{OUT}) on BCD outputs, $V_{OUT} - V_{EE}$ (10kΩ resistor in series with output)	11V
Bias voltage (V_{OUT}) on TTL carry output, $V_{OUT} - V_{EE}$ (1.2kΩ resistor in series with output)	11V
Output current from ECL carry output (I_{OUT}) (Note: the device will be destroyed if the ECL output is shorted to the negative rail)	10mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

QUICK REFERENCE DATA

■ Power Supplies V_{CC}	0V
V_{EE}	−5.2V ± 0.25V
■ Range of clock input amplitude	400-800mV p-p
■ Operational temperature range	0°C to +70°C
■ Frequency range with sinusoidal I/P	40-700 MHz (SP8634B)
■ Frequency range with square wave I/P	DC to 700 MHz (SP8634B)

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP 8640A, B & M 200 MHz
SP 8641A, B & M 250 MHz
SP 8642A, B & M 300 MHz
SP 8643A, B & M 350 MHz
SP 8646A, B & M 200 MHz TTL OUTPUTS
SP 8647 A, B & M 250 MHz TTL OUTPUTS

UHF PROGRAMMABLE DIVIDERS ÷10/11

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8640 series are UHF integrated circuits that can be logically programmed to divide by either 10 or 11, with input frequencies up to 350 MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

Inputs and outputs are ECL compatible throughout the temperature range: the clock inputs and programming inputs are ECL III compatible while the two complementary outputs are ECL II compatible to reduce power consumption in the output stage. ECL 10K output compatability can be achieved very simply however (see Operating Notes). The SP8646/7 feature an additional TTL compatible output.

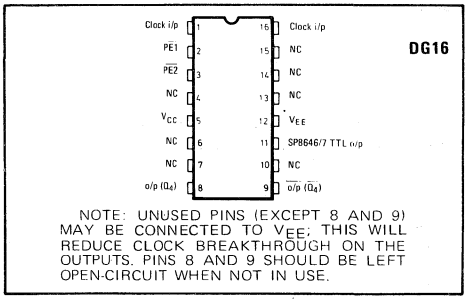
The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either $\overline{PE}$ input is in the high state and by 11 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).

FEATURES

- Military and Industrial Variants.
- 350 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs
- Optional TTL Output

QUICK REFERENCE DATA

- Full Temperature Range Operation:
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.



NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE.

Fig. 1 Pin connections (top)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\|V_{CC} - V_{EE}\|$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	—55°C to +175°C

Clock Pulse	Q_1	Q_2	Q_3	Q_4	TTL O/P
1	L	H	H	H	H
2	L	L	H	H	H
3	L	L	L	H	H
4	H	L	L	H	H
5	H	H	L	H	H
6	L	H	H	L	L
7	L	L	H	L	L
8	L	L	L	L	L
9	H	L	L	L	L
10	H	H	L	L	L
11	H	H	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_4 or the H→L transition from $\overline{Q}_4$ is used to clock the stage controlling the ÷10/11. The loop delay is 10 clock periods minus the internal delays of the ÷10/11 circuit.

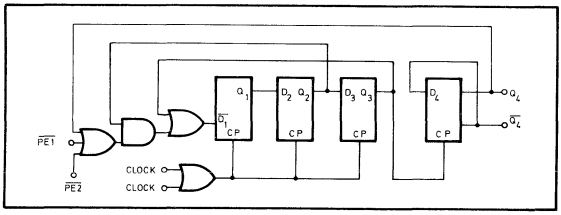


Fig. 2 Logic diagram (positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: −55°C to +125°C (A grade)
−40°C to +85°C (M grade)
0°C to +70°C (B grade)

Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics (all SP8640 series devices)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3.
					I_{out} (external) = 0mA
					(There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES
1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	SP8643	350			MHz	
	SP8642	300			MHz	
	SP8641/7	250			MHz	
	SP8640/6	200			MHz	
Min. frequency with sinewave clock input	All			50	MHz	
Min. slew rate of square wave input for correct operation down to DC	All			100	V/μs	
Propagation delay (clock input to device output)	All		3		ns	ECL Output
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

NOTES

4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse (see Fig. 4).
7. SP8646, SP8647 TTL output current = 8mA at V_{OL} = +0.5V, measured at +25°C, temperature coefficient = +0.5mV/°C
8. SP8646, SP8647 Q_4 to TTL output delay = 3ns, typical
9. The TTL O/P is a free collector and requires a 2k Ω (typ) pull-up resistor. The current taken by this resistor must be included in the 8mA current in Note 7 above.

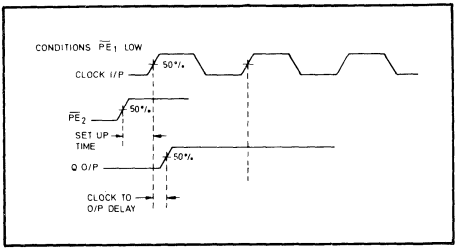


Fig. 3 Set-up timing diagram

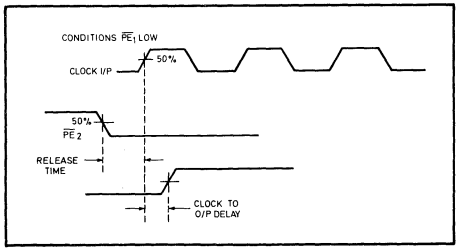


Fig. 4 Release timing diagram

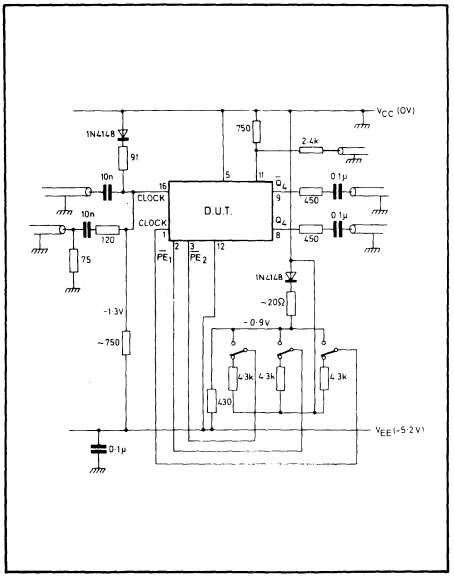


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8640 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

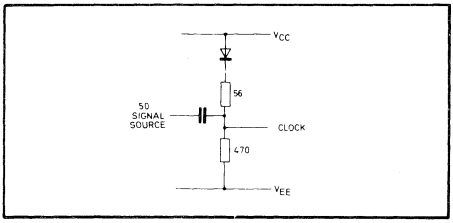


Fig. 6 Recommended input bias configuration for capacitive coupling to a contiruous 50Ω signal source.

The ÷10/11 can be controlled by a TTL fully programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface has been provided on chip in the SP8646/7. A discrete interface may be constructed as shown in Fig. 7. Both output interfaces will operate satisfactorily over the full military temperature range (−55°C to +125°C). The propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10 ns. At an input frequency of 350 MHz this would only leave about 16 ns for the fully-programmable counter to control the ÷10/11. The loop delay can be increased by extending the ÷10/11 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

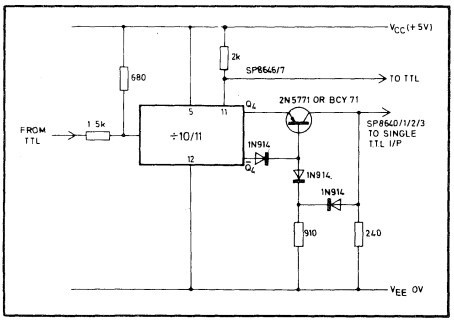


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8640 devices and TTL operating from the same supply rails)

The SP8640 device ECL o/ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

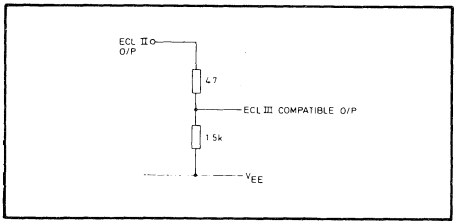


Fig. 8 ECL II to ECL III interface

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8650A, B & M 600MHz÷16
SP8651A, B & M 500MHz÷16
SP8652A, B & M 400MHz÷16

The SP8650 series of UHF ÷ 16 counters are fixed ratio synchronous emitter coupled logic counters with, in the case of the SP8650, a maximum operating frequency in excess of 600MHz. All three devices operate up to their maximum specified operating frequencies over temperature ranges of —55°C to +125°C ('A' grade), 0°C to +20°C ('B' grade) and —40°C to +85°C ('M' grade). The input is normally capacitively coupled to the signal source but the circuits can be DC driven if required. The inputs can be either single driven relative to the on-chip reference voltage or differentially driven.

There are two complementary emitter follower outputs.

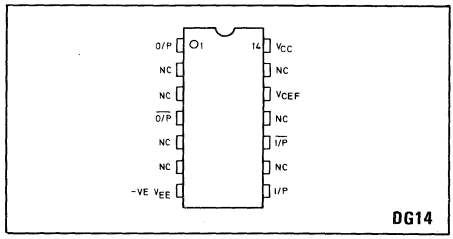


Fig. 1 Pin connections

FEATURES

- Low Power - Typically 250mW
- ECL II & ECL III Output Compatability
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

QUICK REFERENCE DATA

- Power Supplies $V_{CC} = 0V$
  $V_{EE} = -5.2V \pm 0.25V$
- Temperature Range 'A' grade —55°C to +125°C
  'B' grade 0°C to +70°C
  'M' grade —40°C to +85°C
- Input Amplitude Range 400mV to 800mVp-p
- Output Voltage Swing 800mV typ. p-p

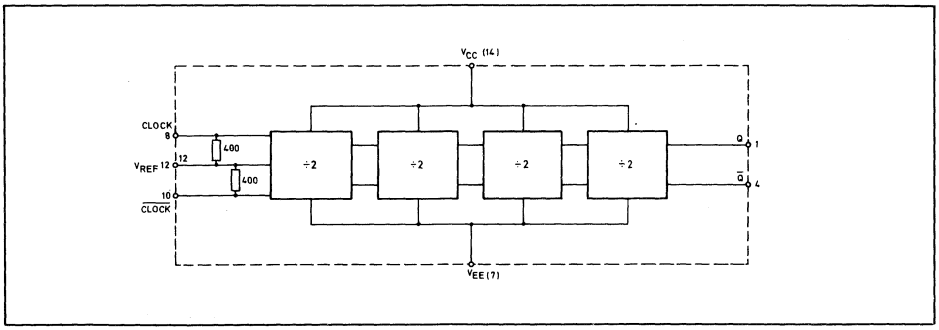


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

T_{amb} = −55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
−40°C to +85°C ('M' grade)

Supply Voltage
V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V

Output load = 500Ω in parallel with approx. 3pF

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
						Test circuit as in fig. 2
Max. Toggle frequency	SP8650	600			HMz	V_{IN} = 400 to 800mV p-p
	SP8651	500			MHz	V_{IN} = 400 to 800mV p-p
	SP8652	400			MHz	V_{IN} = 400 to 800mV p-p
Min. toggle frequency for correct operation with a sinewave input	All			40	MHz	VIN = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to OHz	All			100	V/µs	
Input reference voltage	All		2.6		V	
Output voltage swing (dynamic)	All	500	800		mV	p-p
Output voltage (static)						
high state	All	−8.95		.615	V	
Low state	All	−1.83		−1.435	V	
Power supply drain current	All		45	60	mA	

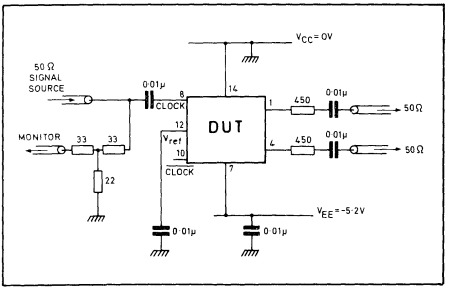


Fig. 3 Toggle frequency test circuit

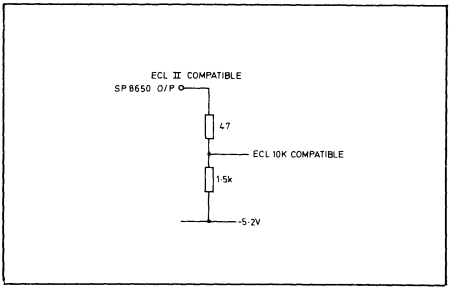


Fig. 4 SP8650 to ECL 10K interface

Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and induction.
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

ABSOLUTE MAXIMUM RATINGS

Power supply voltage /V_{CC} − V_{EE}/		8 volts
Input voltage	V_{INac}	2.5V p-p
Output source curr	I_{out}	10mA
Storage temperature range		−55°C to +125°C
Operating junction temperature		150°C max.

OPERATING NOTE

Normal UHF layout techniques should be used if the SP8650 series of dividers are to operate satisfactorily. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

The device will also miscount if the input transitions are slow — a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8650 series devices would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division rate is optimum where power is at a premium and so the SP8650 series would normally be used in low power applications.

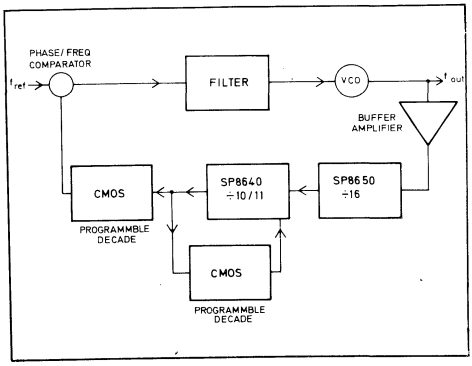


Fig. 5 A low power synthesiser loop

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8655A, B & M (÷32)
SP8657A, B & M (÷20)
SP8659A, B & M (÷16)

The SP8655A, B & M, SP8657A, B & M and SP8659A, B & M are fixed ratio (divide by 32, 20 and 16) low power counters for operation at frequencies in excess of 200 MHz over the temperature ranges −55°C to +125°C ('A' grade), 0°C to+ 70°C ('B' grade) and −40°C to +85°C ('M' grade).

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

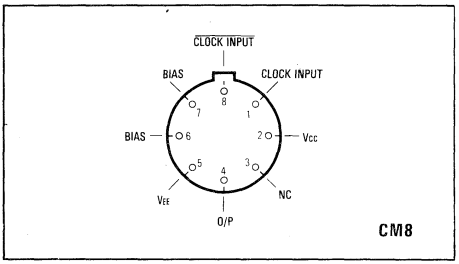


Fig. 1 Pin connections (viewed from beneath)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, V_{CC}—V_{EE}	8V
Input voltage V_{in}	Not greater than supply voltage in use
Output sink current, I_O	10mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

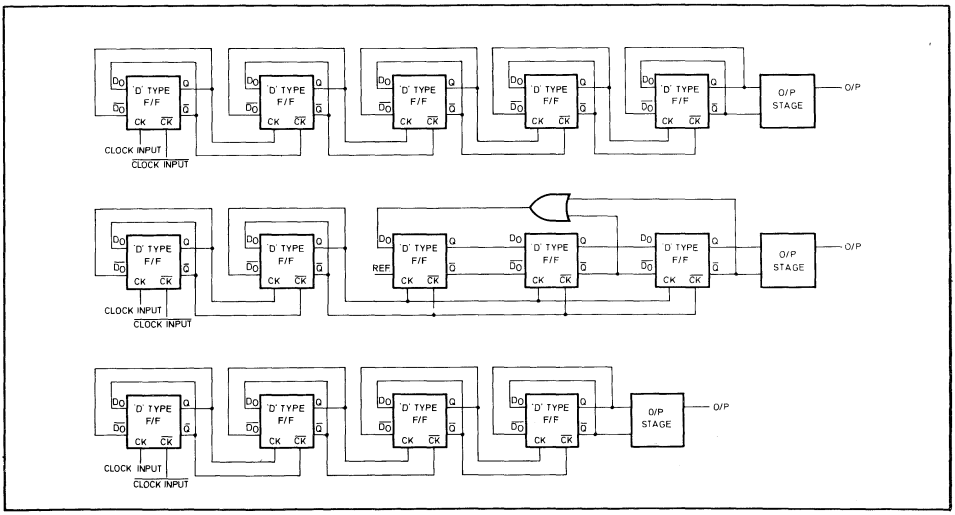


Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating ambient temperature T_{amb}: —55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
—40°C to +85°C ('M' grade)

Operating supply voltages V_{CC}: +5.2V±0.25V; V_{EE}: OV

Input voltage single drive: 400mV to 800mV p-p

double drive: 250mV to 800mV p-p

Output load 3.3k Ω to +10V, in parallel with 7pF.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency	200			MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μs	
Power supply drain current		10	13	mA	V_{CC}=+5.2V
Output level (high)	9.0			V	
Output level (low)			400	mV	

OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39k Ω pulldown resistor from either input (double drive) to V_{EE}; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3k Ω (or less) to a +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

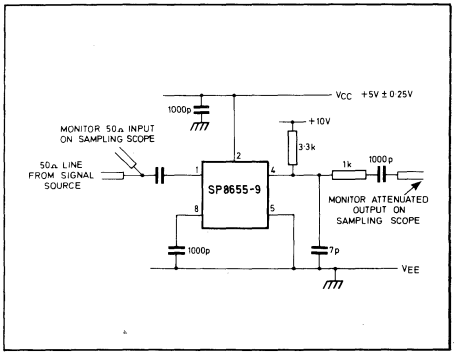


Fig. 3 Test circuit

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8660 A, B & M
180 MHz ÷ 10 (LOW POWER)

The SP8660 is a fixed ratio (divide by 10) low power counter for operation at frequencies in excess of 100MHz over the temperature ranges −55°C to +125°C ('A' grade) 0°C to +70°C ('B' grade) and −40°C to +85°C ('M' grade)

The input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used, the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should also be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

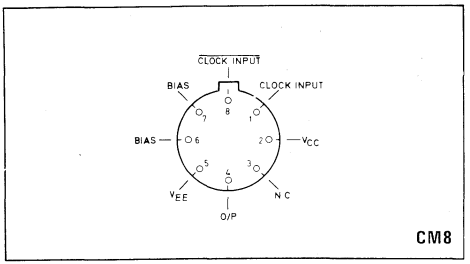


Fig. 1 Pin connections (viewed from beneath)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible
- Military and Commercial Temperature Ranges

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{in}	Not greater than supply voltage in use
Output sink current, I_o	10mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The device will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ pulldown resistor from either input (double drive) to V_{EE}; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ (or less) to +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

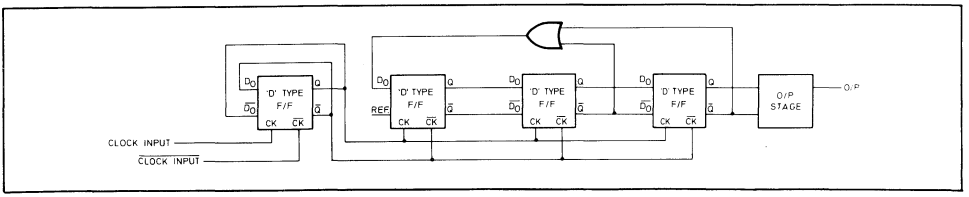


Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Operating ambient temperature T_A

'A' grade: −55°C to +125°C; 'B' grade: 0°C to 70°C; 'M' grade: −40°C to +85°C;

Operating supply voltages

V_{CC} : +5.0V± 0.25V; V_{EE} : 0V

Input voltage

Single drive: 400mV to 800mV p-p; double drive: 250mV to 800mV p-p

Output load 3.3kΩ to +10V, in parallel with 7pF

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Maximum input frequency	100	200		MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μs	
Power supply drain current		10	13	mA	V_{CC} = +5.0V
Output level (high)	9.0			V	
Output level (low)			400	mV	

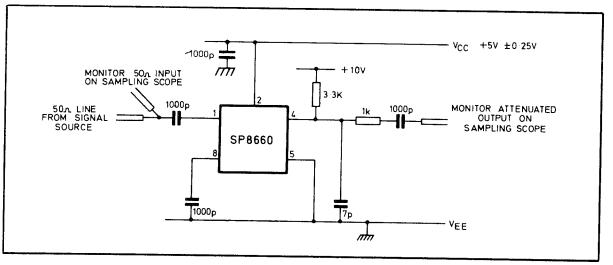


Fig. 3 Test circuit

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

UHF DECADE COUNTERS

SP8665B 1.0GHz ÷ 10 SP8666B 1.1GHz ÷ 10

SP8667B 1.2GHz ÷ 10

The SP8665/6/7 high speed decade counters operating at an input frequency of up to 1GHz over the temperature range 0°C to +70°C.

The device has a typical power dissipation of 550mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input to V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8665/6/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8665/6/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

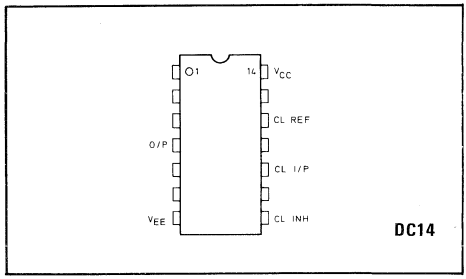


Fig. 1 Pin connections

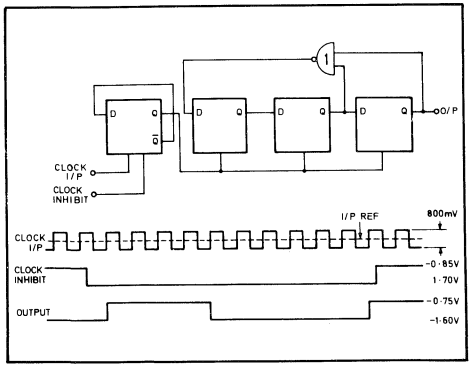


Fig. 2 Logic diagram

FEATURES

- Guaranteed operation over large temperature range 0°C to 70°C
- Wide input dynamic range
- Self biasing clock input
- Clock inhibit input for direct gating capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage inhibit input	V_{EE} to V_{CC}
Input voltage CP input	2.5V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to 150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Supply voltage	6.8V ± 0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T_{amb}	0°C to +70°C
Supply voltage	V_{CC} = 0V V_{EE} = −6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristics		Value			Units	Conditions
		Min.	Typ.	Max.		
Max. i/p frequency	SP8665	1.0			GHz	400mV to 1.2V p-p
	SP8666	1.1			GHz	600mV to 1.2V p-p
	SP8667	1.2			GHz	600mV to 1.2V p-p
Min. i/p frequency				200	MHz	Sine wave input 400mV p-p
Min. i/p frequency				100	MHz	Sine wave input 600mV p-p
Min. slew rate for square wave input				200	V/μsec	
Clock i/p impedance			400		Ω	At low frequency
Inhibit input reference level			−1.3		V	At 25°C compatible with ECL III throughout the temperature range.
Inhibit input pulldown resistor (internal)			6		kΩ	
Output pulldown resistor (internal)			3		kΩ	
Power supply drain current			80	105	mA	At 25°C

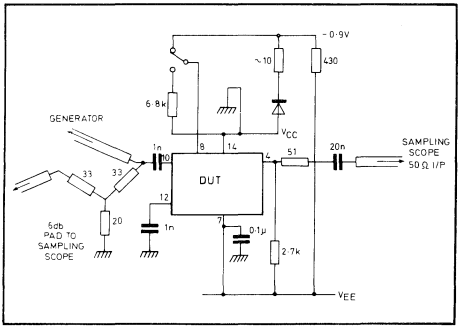


Fig. 3 Test circuit

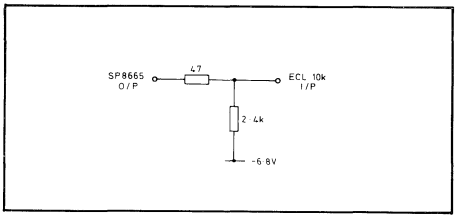


Fig. 4 SP8665 to ECL 10K

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8670 A, B&M 600MHz ÷8
SP8671 A, B&M 500MHz ÷8
SP8672 A, B&M 400MHz ÷8

The SP8670, SP8671 and SP8672 are fixed ratio –8 asynchronous ECL counters with a maximum operating frequency of 600, 500 and 400 MHz respectively. The operating temperature is specified by the final coding letter: –55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade) and –40°C to +85°C ('M' grade). The input is normally capacitively coupled to the signal source but the circuit can be DC driven if required. The inputs can be either single driven, relative to the on-chip reference voltage, or driven differentially. There are two complementary emitter-follower outputs.

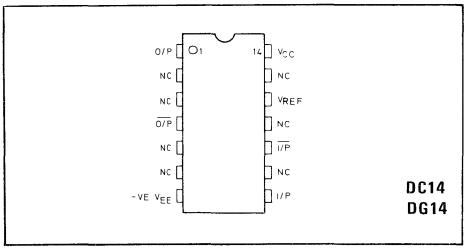


Fig. 1 Pin connections

FEATURES

- Low Power – Typically 250mW
- ECL II & ECL III Output Compatibility
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

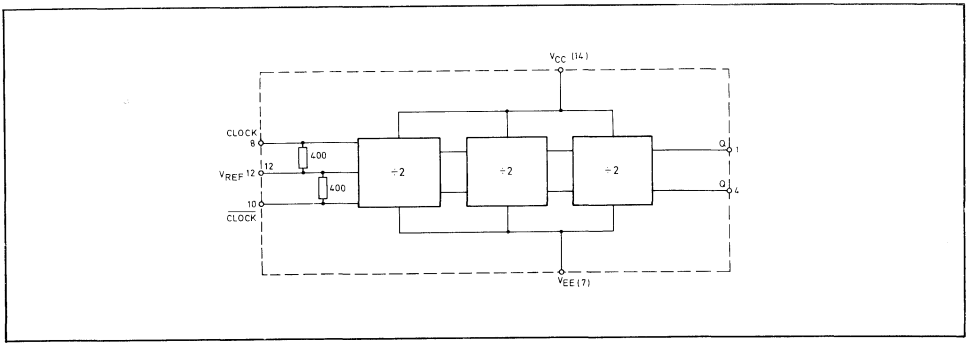


Fig. 2 Functional diagram

QUICK REFERENCE DATA

■	Power Supplies	V_{CC} = 0V V_{EE} = –5.2V ± 0.25V
■	Input Amplitude range	400mV to 800mV p-p
■	Output Voltage Swing	800mV typ. p-p
■	Temp. Ranges:	–55°C to +125°C ('A' Grade) 0°C to +70°C ('B' Grade) –40°C to +85°C ('M' Grade)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

T_{amb} = 'A' grade: −55°C to +125°C;
Supply Voltage 'B' grade: 0°C to 70°C;
V_{CC} = 0V 'M' grade: −40°C to +85°C;
V_{EE} = −5.2V ± 0.25V
Output load = 500Ω line in parallel with approx. 3pF

Characteristic		Value			Units	Condition
		Min.	Typ.	Max.		
Max. Toggle frequency	SP8670	600			MHz	
	SP8671	500			MHz	Test circuit as in fig. 2
	SP8672	400			MHz	V_{IN} = 400 to 800mV p-p
Min. Toggle frequency for correct operation with a sinewave input				40	MHz	V_{IN} = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to 0Hz				100	V/μs	
Input reference voltage			2.6		V	
Output voltage swing (dynamic)		500	800		mV	p-p
Output voltage (static)						
High state		−8.95		.615	V	
Low state		−1.83		−1.435	V	
Power supply drain current			45	60	mA	

Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and inductance
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

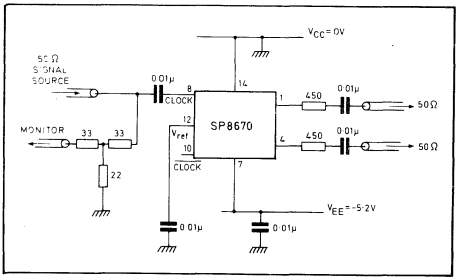


Fig. 3 Toggle frequency test circuit

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

V_{ref} must be decoupled to RF earth by a capacitor in the range 30pF to 1000pF. It is important that this decoupling is adequate, otherwise input sensitivity will be reduced.

The device will also miscount if the input transitions are slow — a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SL8670 would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division ratio is optimum where power is at a premium and so the SP8670 series would normally be used in low power applications.

OPERATING NOTE

Normal UHF layout techniques should be used to ensure satisfactory operation. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

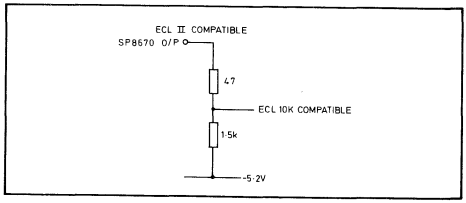


Fig. 4 SP8670 to ECL 10K interface

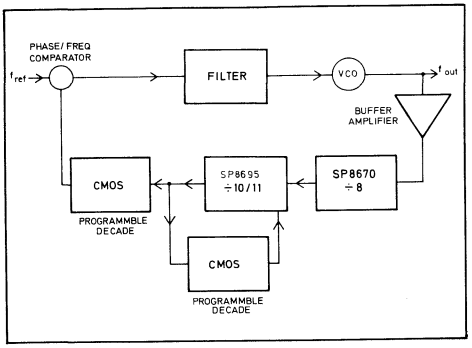


Fig. 5 A low power synthesiser loop

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8 volts
Input voltage V_{INac}	2.5V p-p
Output source current I_{out}	10mA
Storage temperature range	−55°C to +125°C
Operating junction temperature	150°C max.

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES

HIGH SPEED DIVIDERS

SP8675B&M 1.0GHz ÷8
SP8676B&M 1.1GHz ÷8
SP8677B&M 1.2GHz ÷8

The SP8675/6/7 are high speed counters for operation at input frequencies up to 1.2GHz.

The devices have a typical power dissipation of 470mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8675/6/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8675/6/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

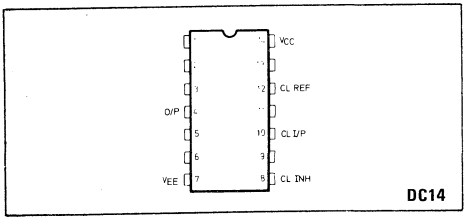


Fig. 1 Pin connections

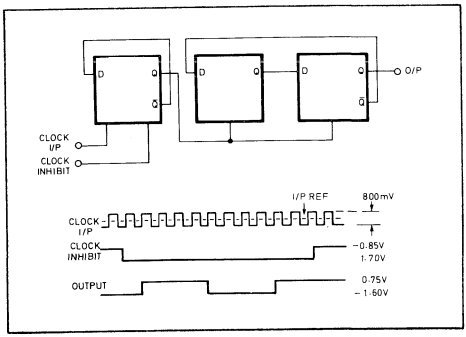


Fig. 2 Logic diagram and timing

FEATURES

- Guaranteed Operation over Large Temperature Range: 'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Wide Input Dynamic Range
- Self Biasing Clock Input
- Clock Inhibit Input for Direct Gating
- Capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC}—V_{EE} 0 to 10V
Input voltage inhibit input V_{EE} to V_{CC}
Input voltage CP input 2.5V p-p
Output current 20mA
Operating junction temperature +150°C
Storage temperature —55°C to +150°C

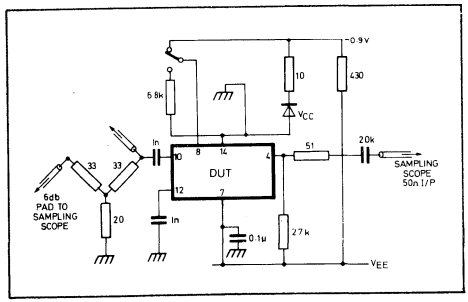


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Supply voltage	6.8V ±0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T_{amb} 'B' grade	0°C to +70°C (see note 1)
'M' grade	−40°C to +85°C (see note 1)
Supply voltage	V_{CC} = OV V_{EE} = −6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency SP8675	1.0			GHz	400mV to 1.2V p-p
SP8676	1.1			GHz	600mV to 1.2V p-p
SP8677	1.2			GHz	600mV to 1.0V p-p
Min i/p frequency			200	MHz	Sine wave input 400mV p-p
			150	MHz	Sine wave input 600mV p-p
Min slew rate for square wave input			200	V/µsec	
Clock i/p impedance		400		Ω	At low frequency
Inhibit input reference level		−1.3		V	At 25°C compatible with ECL III throughout the temperature range
Inhibit input pulldown resistor (internal)		6		kΩ	
Output pulldown resistor (internal)		3		kΩ	
Power supply drain current		70	95	mA	at 25°C

NOTES

1. The SP8677M is tested at T_{case} = −40°C to +85°C. The SP8677M requires a suitable heatsink to be connected during operation.

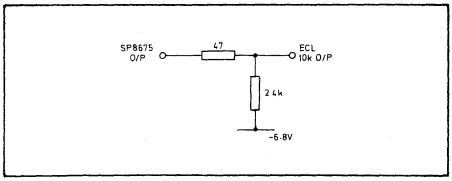


Fig. 4 SP8675 to ECL10K interface

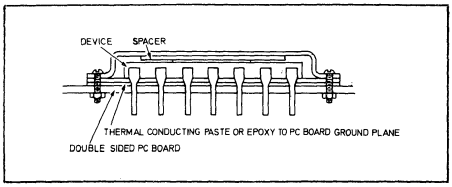


Fig. 5 Heat sink for 'M' grade devices

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8685 A, B&M
UHF PROGRAMMABLE DIVIDER 500MHz ÷ 10/11

The SP8685 A, B & M are high speed programmable – 10/11 counters operating at an input frequency of up to 500 MHz over the temperature ranges -55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade) and -40°C to +85°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either input is in the high state, and by 11 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-ten prescaler the inverse output (o/p) should be connected to a PE input.

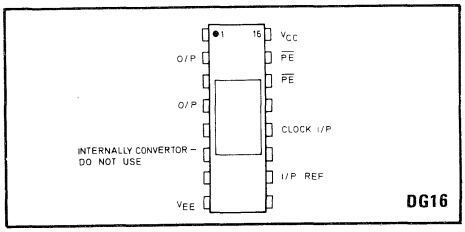


Fig. 1 Pin connections

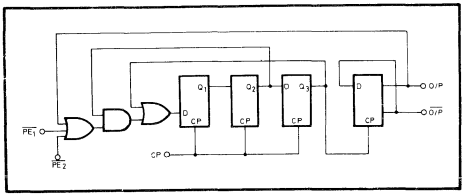


Fig. 2 Logic diagram SP8685

Clock Pulse	Q_1	Q_2	Q_3	Q_4
1	L	H	H	H
2	L	L	H	H
3	L	L	L	H
4	H	L	L	H
5	H	H	L	H
6	L	H	H	L
7	L	L	H	L
8	L	L	L	L
9	H	L	L	L
10	H	H	L	L
11	L	H	H	H

Table 1 Count sequence Extra state

$\overline{PE_1}$	PE_2	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

FEATURES

- Full temperature range operation:
  'A' grade -55°C to +125°C
  'B' grade 0°C to +70°C
  'M' grade -40°C to +85°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	–55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible

Outputs – ECL II compatible

Test conditions (unless otherwise stated)

Tamb 'A' grade -55°C to +125°C
'B' grade 0°C to +70°C
'M' grade -40°C to +85°C

Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	500			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slow rate for square wave input			100	V/μs	
Propogation delay					
(clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown					
Resistors		4.3		KΩ	
Clock i/p impedance					
(i/p to i/p ref low frequency)		400		Ω	

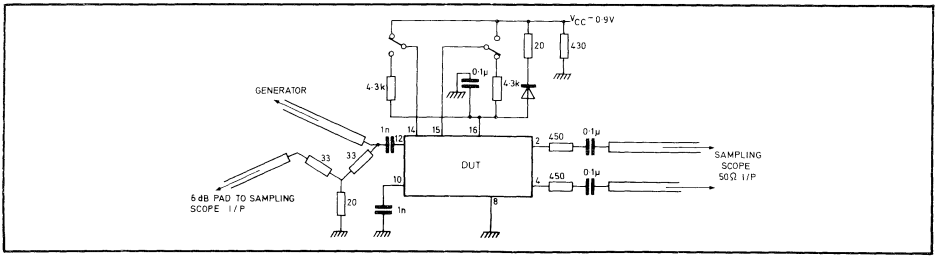


Fig. 3 Test circuit

APPLICATION NOTES

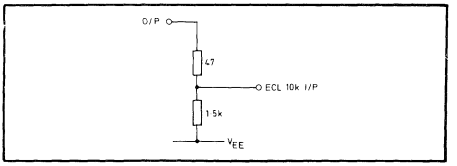


Fig. 4 SP8685 output – ECL 10K i/p and ECLII (or ECL 10K o/ps unloaded) – ECL 10K i/p

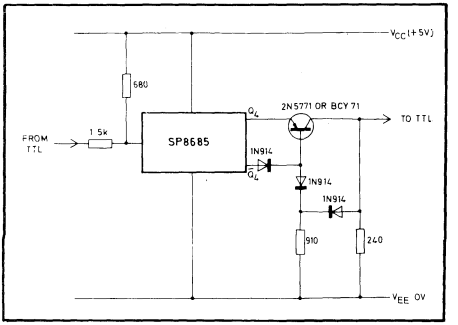


Fig. 5 TTL o/p – SP8685 $\overline{PE}$ i/p; SL8685 o/p – TTL i/p. (Total delay from SP8685 clock i/p to Schottky gate o/p = 15ns, typ.)

At an input frequency of 500 MHz the control loop delay time (SP8685 o/p to PE i/p) is approximately 16 ns. This will be a severe problem if TTL is used in the control loop.

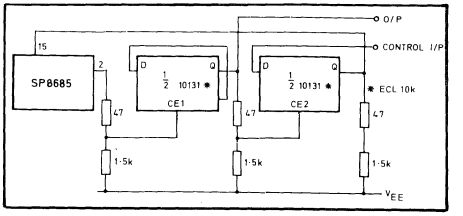


Fig. 6 Divide-by-20/22. Control loop delay time approximately 40ns.

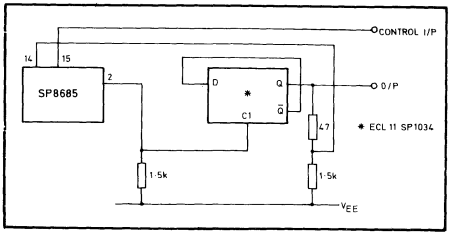


Fig. 7 Divide-by-20/21. Control loop delay time approximately 30ns using SP1034.

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8690 A, B & M 200 MHz ÷ 10/11
AC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8690 A, B & M are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over three temperature ranges: 'A' grade is —55 C to +125 C and the 'B' grade is 0 C to +70 C and the 'M' grade is —40 C to +85 C.

The clock inputs can be either single or differentially driven and must be AC-coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present; to prevent this, a 68kΩ resistor should be connected from pin 1 or 16 to 0V. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed ÷10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

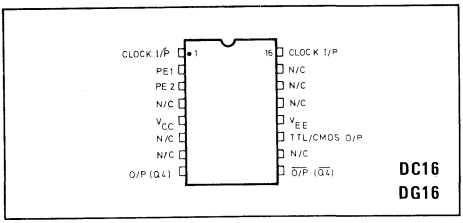
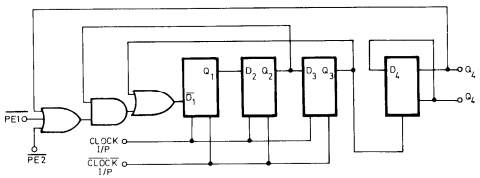


Fig.1 Pin connections

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55 °C to +125 °C
  - 'B' Grade 0 °C to +70 °C
  - 'M' Grade —40 °C to +85 °C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 70mW Typical
- ECL Compatibility on All Inputs
- Capacitively Coupled Clock Input for Synthesiser and Counter Applications
- True and Inverse Outputs Available with ECL Compatibility
- Output Available for Driving TTL or CMOS



Division ratio				
I/P	11	10	10	10
$\overline{PE1}$	L	H	L	H
$\overline{PE2}$	L	L	H	H

Count sequence				
Q_1	Q_2	Q_3	Q_4	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	
H	H	H	H	Extra state

Fig.2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C

Supply voltage V_{CC} = +5V ±0.25V
V_{EE} = 0V
Clock I/P voltage 400mV to 800mV peak to peak
Pin 16 (decoupled to 0V)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		15		MHz	
Min. slew rate of square wave I/P for correct operation		40		V/µs	
$\overline{PE}$ input levels					
V_{INH}	+4.1		+4.5	V	V_{CC}=+5V
V_{INL}	0.0		+3.5	V	T_{amb}=+25°C (note 1)
Q4 & $\overline{Q4}$ output voltage levels					T_{amb}=+25°C (note 2)
V_{OH}	4.15			V	I_{out} (external) = 0mA
V_{OL}			+3.5	V	(There is internal circuitry equivalent to a 3.8kΩ pulldown resistor on each output)
TTL/CMOS output voltage levels					
V_{OL}			+0.4	V	Sink current 3.2mA on
V_{OH}	see note 3				TTL output
Input pulldown resistors between input pins 2 & 3 and −ve rail		10		kΩ	
Power supply drain current		14		mA	V_{CC}=+5V; T_{amb}=25°C
Impedance of clock I/P		1.6		kΩ	in=0Hz
Clock to TTL output delay (O/P −ve going)		22		ns	8mA sink current
Clock to TTL output delay (O/P −ve going)		8		ns	TTL output
Clock to ECL output delay		6		ns	
Set up time		2		ns	See note 4
Release time		4		ns	See note 5

NOTES
1. The $\overline{PE}$ reference voltage level is compatible with ECL II and ECL 10k over the specified temperature range.
2. The Q_4 and $\overline{Q_4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
3. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.
4. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
5. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

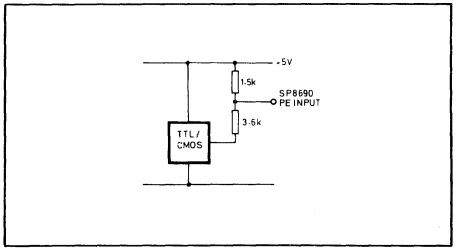


Fig.3 TTL/CMOS interface

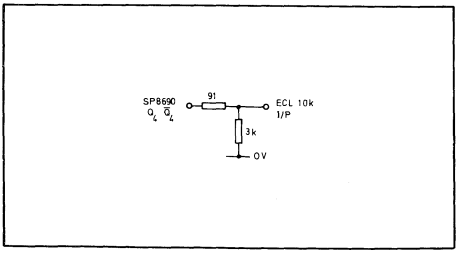


Fig.4 ECL 10K output interface

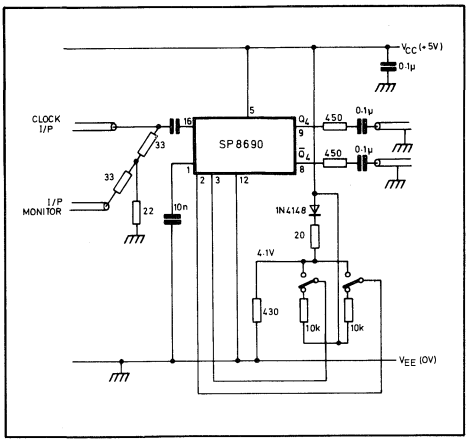


Fig.5 Test circuit for dynamic measurements

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC}—V_{EE}\rvert$	V8
Input voltage V_{IN} d.c.	Not greater than the supply voltage in use
Output current I_{out} (Q_4 & $\overline{Q_4}$)	10mA
Maximum junction temperature	150°C
Storage temperature range	—55°C to +150°C

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8695 A B & M 200 MHz ÷ 10/11
DC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8695 A, B & M are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over two temperature ranges, 'A' grade is —55 °C to +125 °C, the 'B' grade is 0 °C to +70 °C and 'M' grade is —40 °C to +85 °C.

The clock inputs are ECL II, III & 10K compatible throughout the temperature range (see note 1).

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed ÷10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

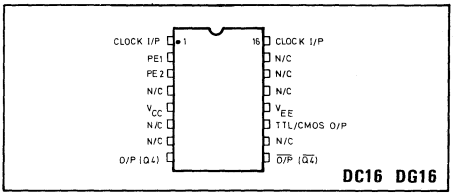
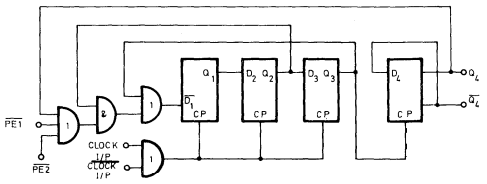


Fig.1 Pin connections

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55 °C to +125 °C
  - 'B' Grade 0 °C to +70 °C
  - 'M' Grade —40 °C to +85 °C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 80mW Typ.
- ECL Compatibility on All Inputs
- Excellent Low Frequency Operation
- True and Inverse Outputs Available with ECL Compatibility.
- Output Available for Driving TTL or CMOS



Division ratio				
I/P	11	10	10	10
$\overline{PE1}$	L	H	L	H
$\overline{PE2}$	L	L	H	H

Count sequence				
Q_1	Q_2	Q_3	Q_4	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	
H	H	H	H	Extra state

Fig.2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C
Supply voltage V_{CC} = −5V ±0.25V
V_{EE} = 0V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		1		MHz	
Min. slew rate of square wave I/P for correct operation		3		V/µs	
Clock I/P voltage levels					
V_{INH}	−4.0		4.2*	V	V_{ref} = +3.8V
V_{INL}	−3.4*		+3.6	V	at T_{amb} = 25°C (note 1)
$\overline{PE}$ input levels					
V_{INH}	−4.1		+4.5	V	T_{amb} = +25°C (note 2)
V_{INL}	0.0		+3.5	V	
Q4 & $\overline{Q4}$ output voltage levels					T_{amb} = +25°C (note 3)
V_{OH}	−4.15			V	I_{out} (external) = 0mA
V_{OL}			+3.5	V	(There is internal circuitry equivalent to 1 3.8kΩ pulldown resistor on each output)
TTL/CMOS output voltage levels					
V_{OL}			+0.4	V	Sink current 3.2mA on TTL output
V_{OH}	see note 4				
Input pulldown resistors between input pins 1, 2, 3 & 16 and −ve rail		10		kΩ	
Power supply drain current		16		mA	V_{CC} = +5V; T_{amb} = +25°C.
Clock to TTL output delay (O/P −ve going)		22		ns	8mA sink current
Clock to TTL output delay (O/P −ve going)		8		ns	TTL output
Clock to ECL output delay		6		ns	
Set up time		2		ns	See note 4
Release time		4		ns	See note 5

NOTES
1. This reference level of −3.8V will enable the clock inputs to be driven from ECL II, III & 10K when their outputs are sinking 3mA. The input reference voltage is compatible with ECL II, III and 10k over the specified temperature range.
2. The $\overline{PE}$ reference voltage level is compatible with ECL II and 10k over the specified temperature range.
3. The Q_4 and $\overline{Q4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
4. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed −12V.
5. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
6. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

*High frequency limits only.

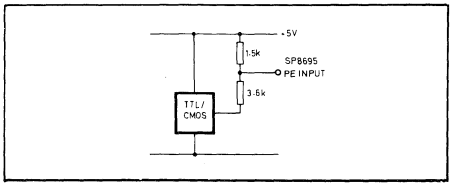


Fig.3 TTL/CMOS interface

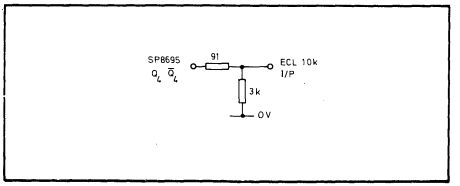


Fig.4 ECL 10K output interface

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}—V_{EE}	V8
Input voltage V_{IN} d.c.	Not greater than the supply voltage in use
Output current I_{out} (Q_4 & Q_4)	10mA
Maximum junction temperature	150 °C
Storage temperature range	—55 °C to +150 °C

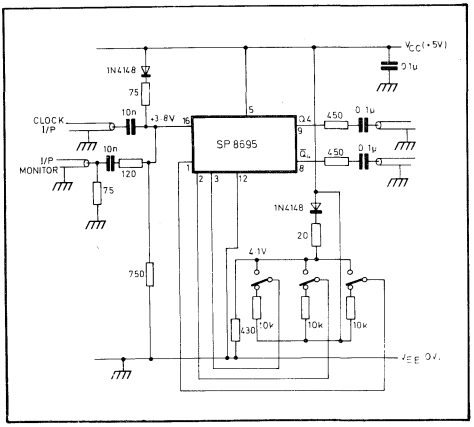


Fig.5 Test circuit for dynamic measurements

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP8735B ÷8 AT 600MHz WITH BINARY OUTPUTS
SP8736B ÷8 AT 500MHz WITH BINARY OUTPUTS

The SP8735B and SP8736B are divide-by-eight circuits with binary outputs for operation from DC up to specified input frequencies of 600 MHz and 500 MHz respectively over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The binary outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10K compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

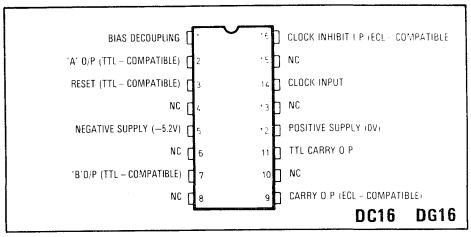


Fig.1 Pin connections (viewed from top)

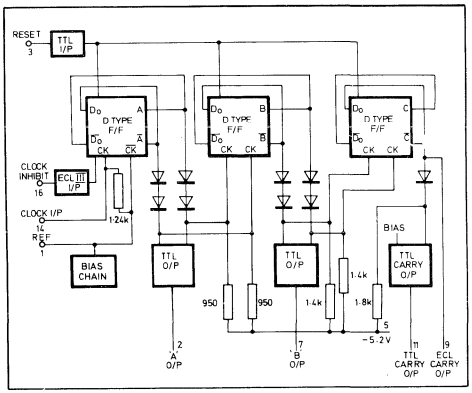


Fig.2 SP8735/6 logic diagram

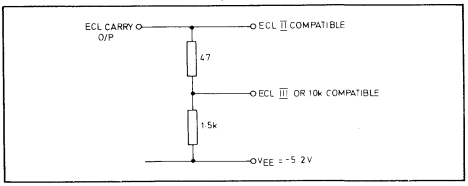


Fig.3 ECL II to ECL 10K interface

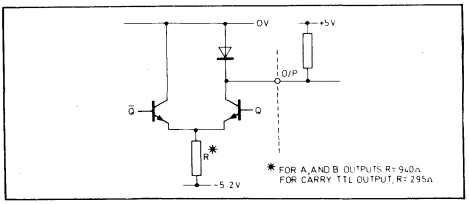


Fig. 4 TTL output circuit diagram

FEATURES

- Direct Gating Capability at up to 600 MHz
- TTL Compatible Binary Outputs
- TTL and ECL Compatible Carry Outputs
- Power Consumption Less Than 450mW
- Wide Dynamic Input Range

APPLICATIONS

- Counters
- Timers
- Synthesisers

QUICK REFERENCE DATA

- Power Supplies : V_{cc} 0V
  V_{ee} −5.2V ± 0.25V
- Range of Clock Input Amplitude : 400 – 800 mV p-p
- Operating Temperature Range :
  0°C to 70°C
- Frequency Range with Sinusoidal I/P : 40 – 600MHz (SP8735)
- Frequency Range with Square Wave I/P : DC to 600MHz (SP8735)

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated):

T_{amb} 0°C to +70°C
Power Supplies V_{CC} OV
V_{EE} −5.2V±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input (pin 14)					
Max. input frequency					
SP8735B	600			MHz	Input voltage 400–800mV p-p
SP8736B	500			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/µs	
Clock inhibit input (pin 16)					
High level (inhibit)	−0.960			V	T_{amb} = +25°C (see note 1)
Low level			−1.650	V	
Edge speed for correct operation at max. clock I/P frequency			2.5	ns	10% to 90%
Reset input (pin 3)					
High level (reset)	See note 2				See note 2
Low level			+0.4	V	
Reset ON time	100			ns	
TTL outputs A & B (pins 2 & 7)					
Output high level	+2.4			V	10k Ω resistor and 3 TTL gate
Output low level			+0.4	V	from O/P to 5V rail (see note 3)
TTL carry output (pin 11)					
Output high level	+2.4			V	5k Ω resistor and 3 TTL gates from O/P to +5V rail
Output low level			+0.4	V	
ECL carry output (pin 9)					
Output high level	−0.975			V	T_{amb} = +25°C
Output low level			−1.375	V	External current = 0mA (See note 4)
Power supply drain current		70	90	mA	V_{EE} − 5.2V

NOTES

1. The clock inhibit input levels are compatible with the ECL III and ECL 10K levels throughout the temperature ranges specified.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series devices.
3. These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10k Ω resistors (see Fig. 4).
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

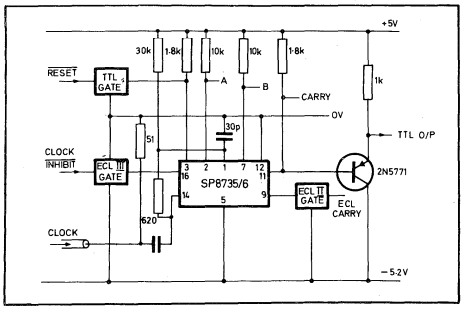


Fig.5 Typical operating diagram

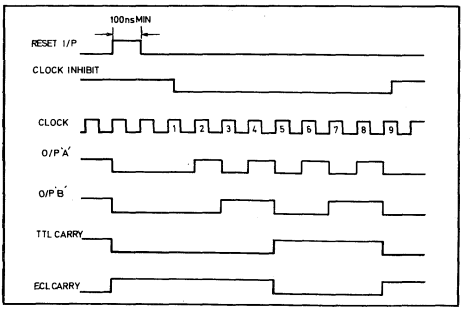


Fig.6 Output waveforms

OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system — the ECL and the decade counter being connected between voltage rails of 0V and —5.2V and the TTL between voltage rails of 0V and +5V. Provided that this is done ECL and TTL compatibility is achieved. (See Figs. 4 and 5)

The clock is normally capacitively coupled to the signal source: a 1000 pF UHF capacitor should be adequate. For low frequency operation, the 1000 pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor — preferably a chip type, but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV p – p. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{cc} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 30Ω resistor between the clock input and the positive supply and a 620Ω resistor between clock and pin 1. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason the input slew rates should be greater than 100V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit will clock the device, provided that the other input is in the low state.

The binary outputs give TTL-compatible outputs (fan out = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the counter and so the state on the TTL outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

A typical application is shown in Fig. 7.

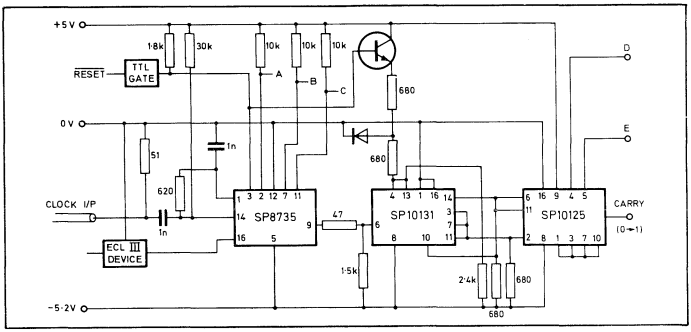


Fig.7 600MHz ÷ 32 with reset and inhibit

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8740 A, B & M
AC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 5/6

The SP8740 A, B & M are high speed programmable ÷5/6 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to +70°C and −40°C to +85°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 5 when either input is in the high state, and by 6 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-five prescaler the inverse output (o/p) should be connected to a PE input.

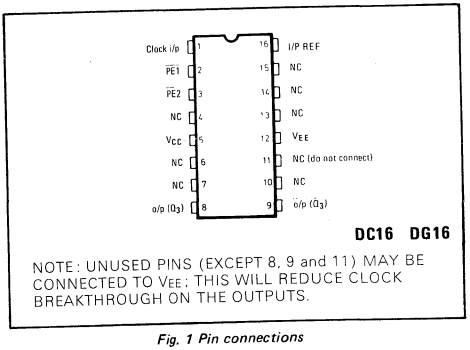


Fig. 1 Pin connections

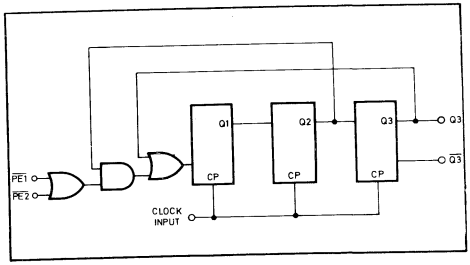


Fig. 2 Logic diagram SP8740

Clock Pulse	Q_1	Q_2	Q_3	
1	L	H	H	
2	L	L	H	
3	L	L	L	
4	H	L	L	
5	H	H	L	
6	H	H	H	← Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Table 2 Truth table for control inputs

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55°C to +125°C
  - 'B' Grade 0°C to +70°C
  - 'M' Grade —40°C to +85°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test conditions (unless otherwise stated)

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C

Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	300			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown Resistors		4.3		KΩ	
Clock i/p impedance (i/p to i/p ref low frequency)		400		Ω	

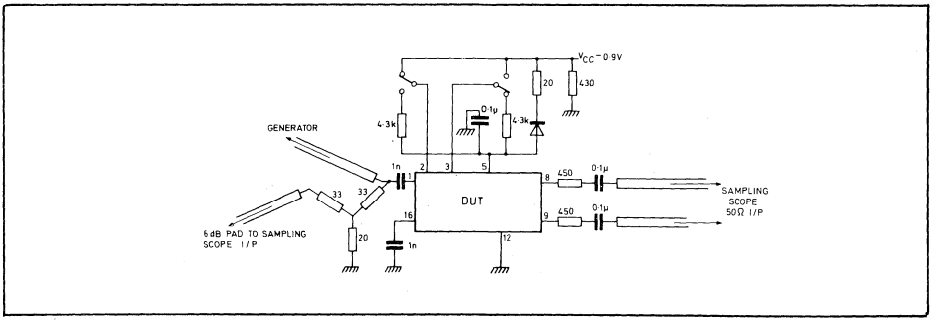


Fig. 3 Test circuit

APPLICATION NOTES

When operating the SP8740 in a synthesiser loop at 300MHz, the delay time through the programmable divider controlling the SP8740 is approximately 13ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

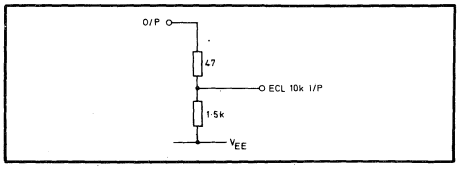


Fig. 4

The simple passive interface from the output of the SP8740 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8740 into TTL, is shown in Fig. 5.

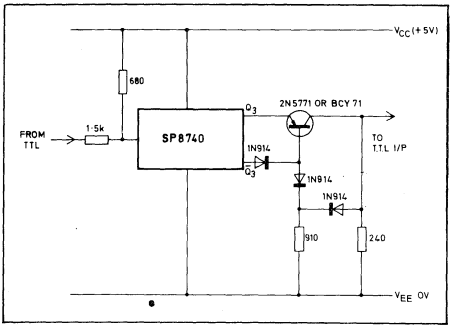


Fig. 5

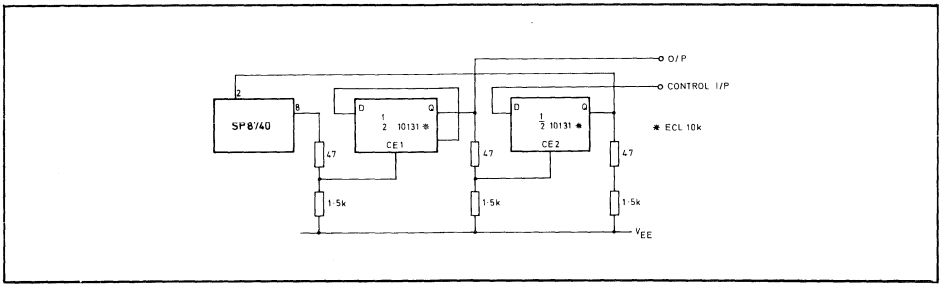


Fig. 6 Divide by 10/12. Control loop delay time approximately 33 ns

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8741 A, B & M
AC COUPLED UHF PROGRAMMABLE DIVIDERS 300 MHz ÷ 6/7

The SP8741 A, B & M are high speed programmable ÷6/7 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to 70°C and −40°C to +85°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 6 when either input is in the high state, and by 7 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

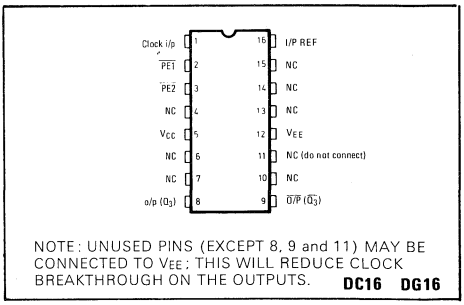
When using the device as a divide-by-six prescaler the inverse output (o/p) should be connected to a PE input.

Clock Pulse	Q_1	Q_2	Q_3	
1	L	H	H	
2	L	L	H	
3	H	L	H	
4	L	H	L	
5	L	L	L	
6	H	L	L	
7	H	H	H	← Extra state

Table 1 Count sequence

$\overline{PE}_1$	$\overline{PE}_2$	Div Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Table 2 Truth table for control inputs



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. **DC16 DG16**

Fig. 1 Pin connections

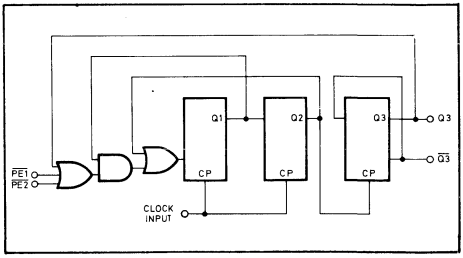


Fig. 2 Logic diagram

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55°C to +125°C
  - 'B' Grade 0°C to +70°C
  - 'M' Grade —40°C to +85°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K — Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test conditions (unless otherwise stated)

T_{amb}: 'A' grade –55°C to +125°C
'B' grade 0°C to +70°C
'M' grade–40°C to +85°C

Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	300			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown Resistors		4.3		KΩ	
Clock i/p impedance (i/p to i/p ref low frequency)		400		Ω	

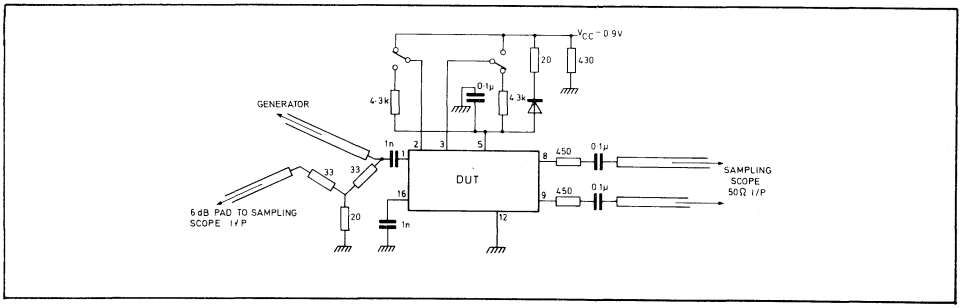


Fig. 3 Test circuit

APPLICATION NOTES

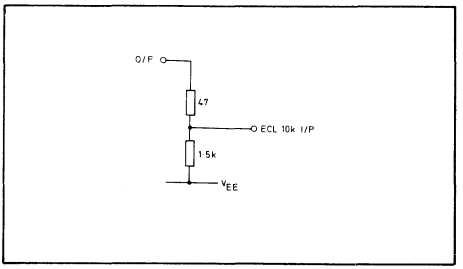


Fig. 4

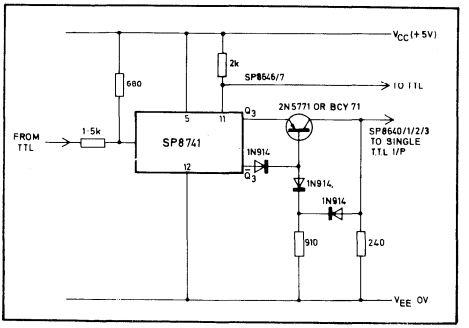


Fig. 5

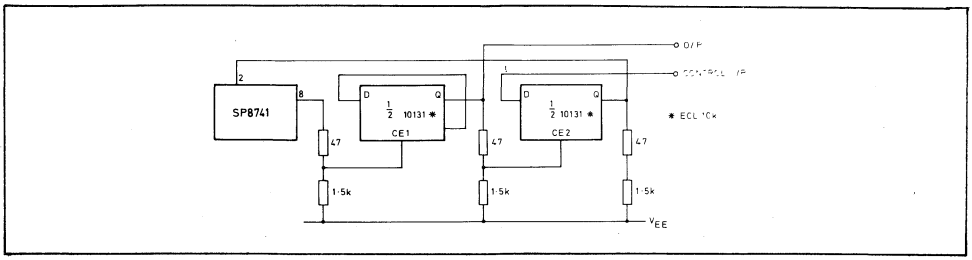


Fig. 6 Divide-by-12/14. Control loop delay time approximately 40ns.

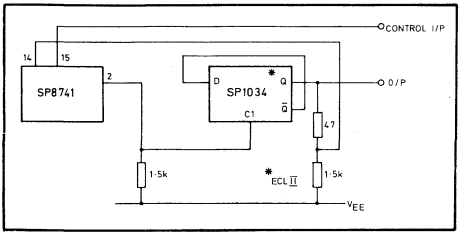


Fig. 7 Divide-by-12/13. Control loop delay time approximately 30ns using SP1034.

When operating the SP8741 in a synthesiser loop at 300MHz the delay time through the programmable divider controlling the SP8741 is approximately 16ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8741 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8741 into TTL, is shown in Fig. 5.

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP 8743 B & M
AC COUPLED UHF PROGRAMMABLE DIVIDER 500 MHz ÷8/9

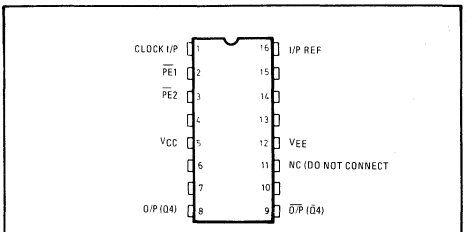
The SP8743M and B are high speed, programmable ÷ 8/9 counters operating at an input frequency of up to 500MHz over the temperature ranges −40°C to +85°C and 0°C to 70°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 8 when either input is in the high state and by 9 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-eight prescaler the inverse output (o/p) should be connected to a $\overline{PE}$ input.



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

DG 16
DC 16

Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage PE inputs	0V to V_{CC}
Input voltage CP input	2V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

FEATURES

- Operating Temperature Range:
  0°C to 70°C ('B' grade)
  −40°C to +85°C ('M' grade)
- Self Biasing Clock Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

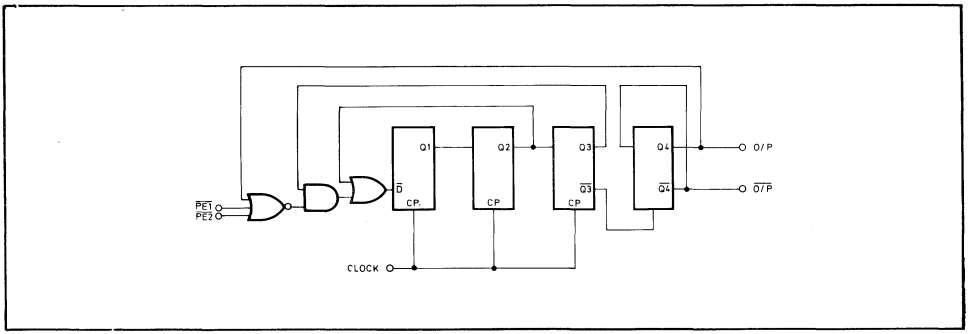


Fig. 2 SP8743 logic diagram

Count Sequence			
Q_1	Q_2	Q_3	Q_4
L	H	H	H
L	L	H	H
H	L	L	L
H	H	L	L
L	H	H	L
L	L	H	L
L	L	L	H ← Extra state
H	L	L	H
H	H	L	H

Division Ratio				
	9	8	8	8
$\overline{PE1}$	L	L	H	H
$\overline{PE2}$	L	H	L	H

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test Conditions (unless otherwise stated):
T_{AMB} 0°C to +70°C ('B' grade) –40°C to +85°C ('M' grade)
Supply Voltage V_{CC} = +5.2V ± 0.25V V_{EE} = 0V
Clock Input Voltage 400mV to 800mV p-p

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	500			MHz	V_{CC} = +5.2V
Min. i/p frequency			40		Sinewave Input
Min. Slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{CC} = +5.2V, 25°C
Power Supply drain current		45	60	mA	V_{CC} = +5.2V, 25°C
$\overline{PE}$ input pulldown resistors		4.3		kΩ	
Clock i/p impedance		400		Ω	
(i/p to i/p ref. low freq.)					

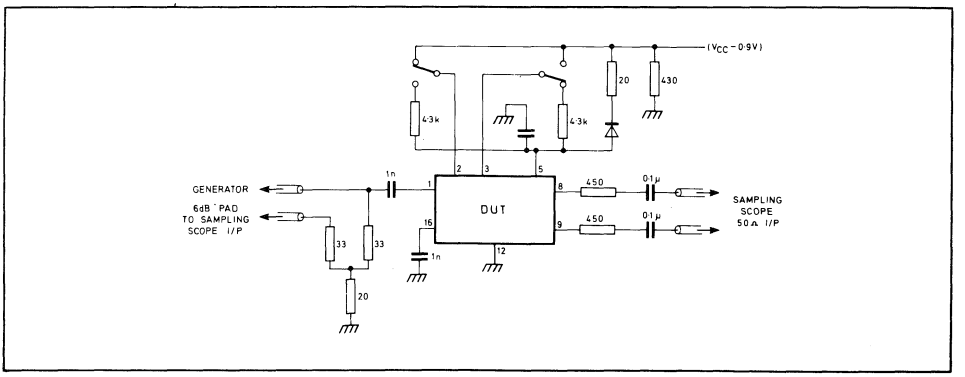


Fig. 3 Test circuit

APPLICATIONS INFORMATION

Interfaces

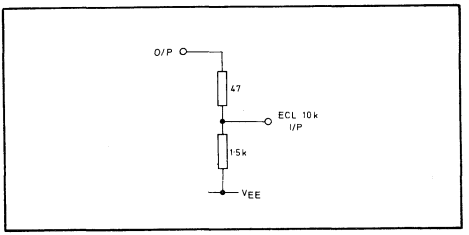


Fig. 4

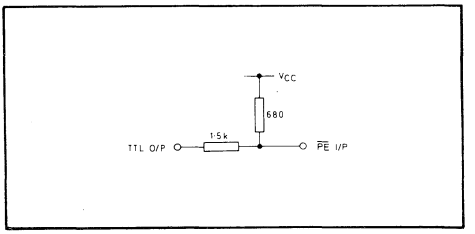


Fig. 5

When operating the SP8743 in a synthesiser loop at 500MHz, the delay time through the programmable divider controlling the SP8743 is approximately 12ns As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8743 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8743 into TTL, is shown in Fig. 5.

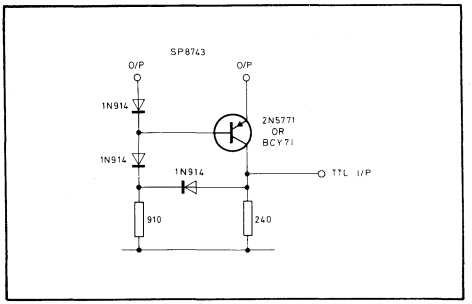


Fig. 6 SP8743 O/P to TTL I/P. Total delay from SP8743 clock I/P to Schottky gate O/P = 15ns typical.

Sub-Systems

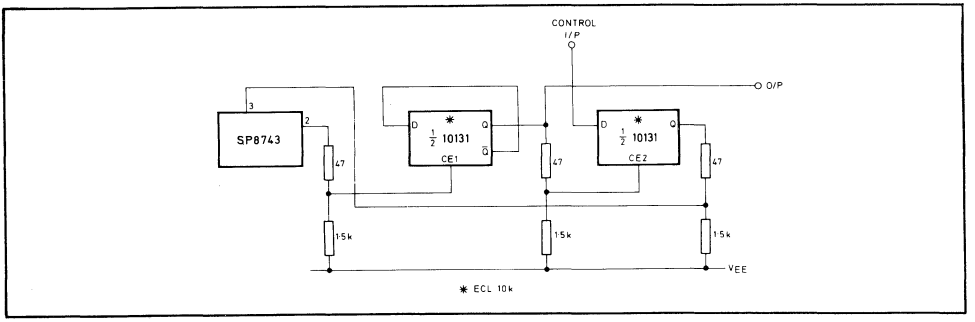


Fig.7 A ÷ 32/33 application. Control loop delay time approx. 56ns.

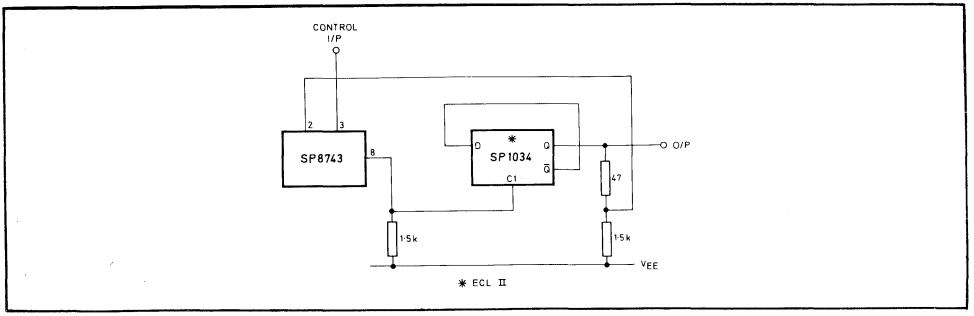


Fig.8 A÷16/17 application. Control loop delay time approx. 24ns using SP1034

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8745 A, B & M
DC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 5/6

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

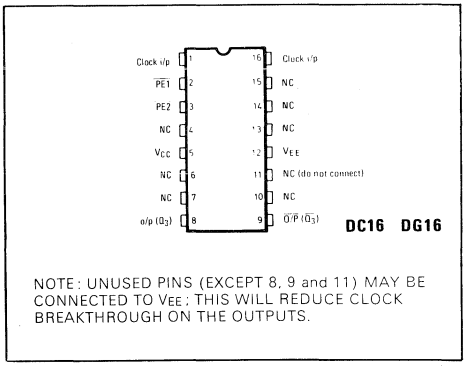
The SP8745 series are UHF integrated circuits that can be logically programmed to divide by either 5 or 6 with input frequencies up to 300 MHz. MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL III-compatible while the two complementary outputs are ECL II-compatible to reduce power consumption in the output stage. ECL III output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 5 when either $\overline{PE}$ input is in the high state and by 6 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3kΩ pulldown resistors to V_{EE} (negative rail)

FEATURES

- Military and Industrial Variants.
- 300 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

Fig. 1 Pin connections (top)

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade −40°C to + 85°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\|V_{CC} - V_{EE}\|$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

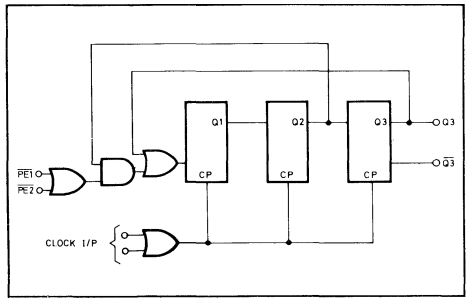


Fig. 2 Logic diagram (positive logic)

Clock Pulse	Q_1	Q_2	Q_3
1	L	H	H
2	L	L	H
3	L	L	L
4	H	L	L
5	H	H	L
6	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L → H transition from Q_3 or the H → L transition from $\overline{Q}_3$ is used to clock the stage controlling the ÷5/6. The loop delay is 5 clock periods minus the internal delays of the ÷5/6 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: (A grade) −55°C to +125°C
(B grade) 0°C to +70°C
(M grade) −40°C to 85°C
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	All	300			MHz	
Min. frequency with sinewave clock input	All			10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz	All			20	V/μs	
Propagation delay (clock input to device output)	All		3		ns	
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

NOTES

4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷5) mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷6 mode is forced by that clock pulse (see Fig. 4).

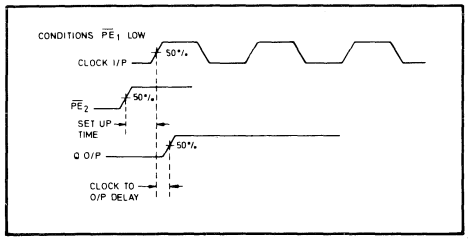


Fig. 3 Set-up timing diagram

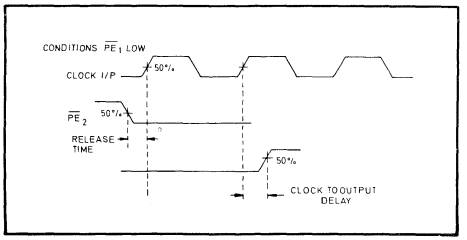


Fig. 4 Release timing diagram

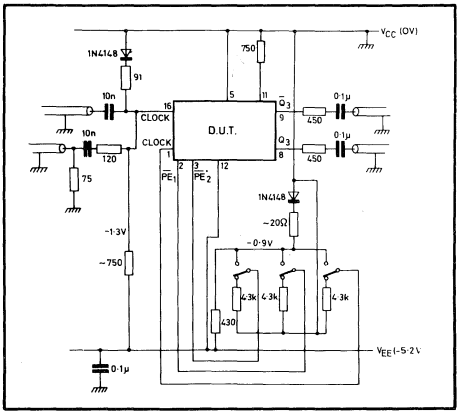


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8745 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig.6, or alternatively an internally biased SP8742.

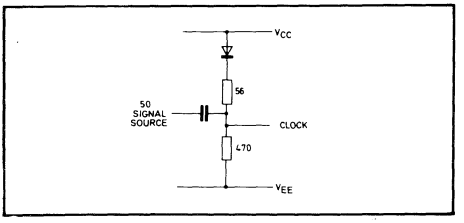


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source.

The ÷5/6 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_3 and $\overline{Q_3}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 300 MHz this would only leave about 6.5ns for the fully-programmable counter to control the ÷5/6. The loop delay can be increased by extending the ÷5/6 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

The SP8745 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

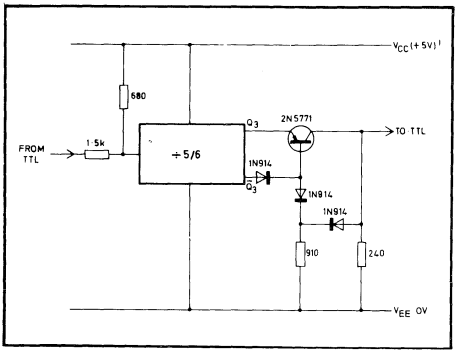


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8745 device and TTL operating from the same supply rails)

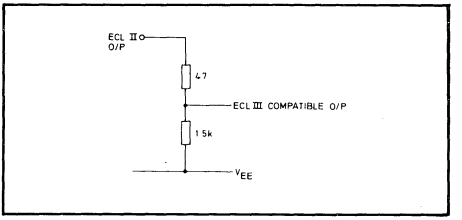


Fig. 8 ECL II to ECL III interface

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8746 A, B & M
DC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 6/7

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8746 series are UHF integrated circuits that can be logically programmed to divide by either 6 or 7, . with input frequencies up to 300 MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL III -compatible while the two complementary outputs are ECL II-compatible to reduce power consumption in the output stage. ECL III output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 6 when either $\overline{PE}$ input is in the high state and by 7 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).

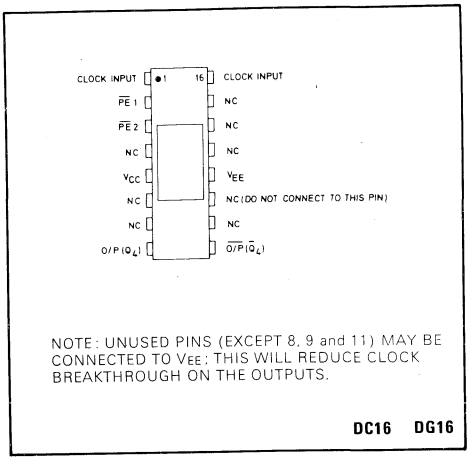


Fig. 1 Pin connections (top)

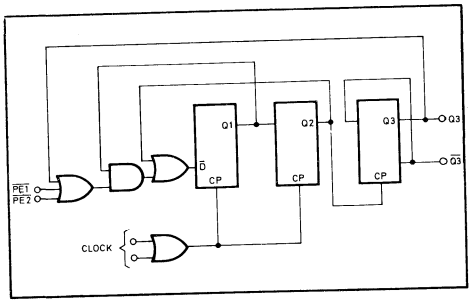


Fig. 2 Logic diagram (positive logic)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{in} (d.c.)	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

FEATURES

- Military and Industrial Variants.
- 300 MHz Toggle Frequency.
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade −40°C to + 85°C
- Supply Voltage
  $\lvert V_{CC} - V_{EE} \rvert$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

Clock Pulse	Q_2	Q_3	Q_4
1	L	H	H
2	L	L	H
3	H	L	H
4	L	H	L
5	L	L	L
6	H	L	L
7	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L → H transition from Q_3 or the H → L transition from $\overline{Q_3}$ is used to clock the stage controlling the ÷6/7. The loop delay is 6 clock periods minus the internal delays of the ÷6/7 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C

Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

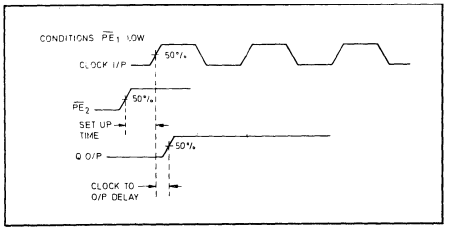


Fig. 3 Set-up timing diagram

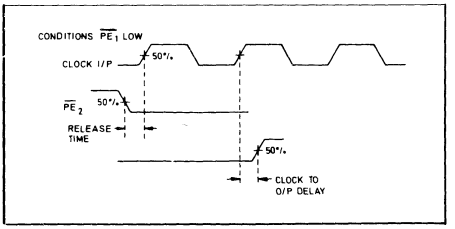


Fig. 4 Release timing diagram

Dynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	All	300			MHz	
					MHz	
					MHz	
					MHz	
Min. frequency with sinewave clock input				10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz				20	V/μs	
Propagation delay (clock input to device output)			3		ns	
Set-up time			1.5		ns	See note 5
Release time			1.5		ns	See note 6

NOTES

4. The devices are dynamically tested using the circuit shown in Fig.5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷6 mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷7 mode is forced by that clock pulse (see Fig. 4).

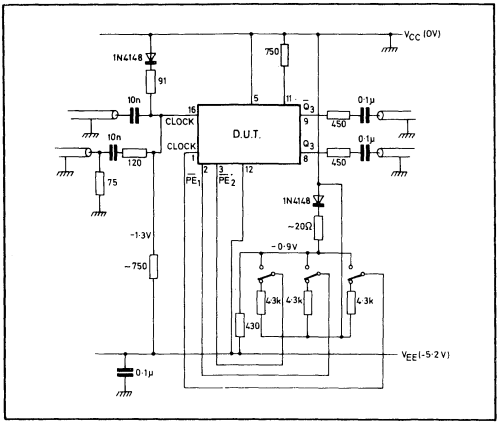


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8746 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control imputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6. Alternatively an SP8741 can be substituted.

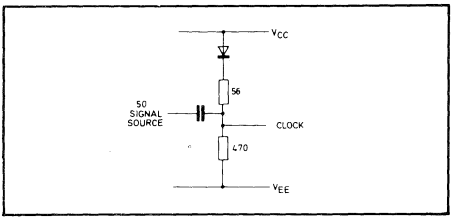


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source.

The ÷6/7 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_3 and $\overline{Q_3}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 300 MHz this would only leave about 10 ns for the fully programmable counter to control the ÷6/7. The loop delay can be increased by extending the ÷6/7 function to, say, ÷24/25 or 48/49 (see Application Notes)

The SP8746 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

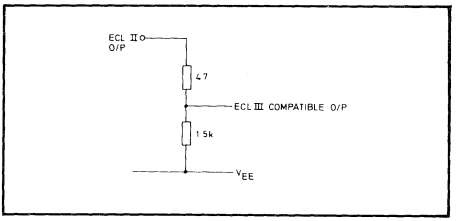


Fig. 8 ECL II to ECL III interface

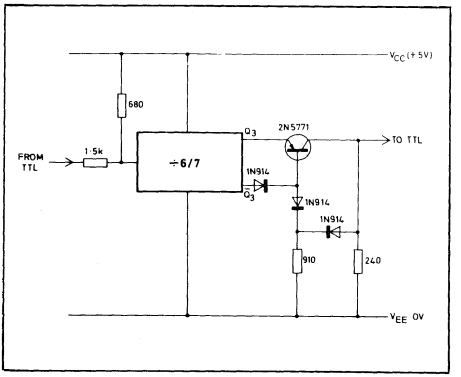


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8746 devices and TTL operating from the same supply rails)

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

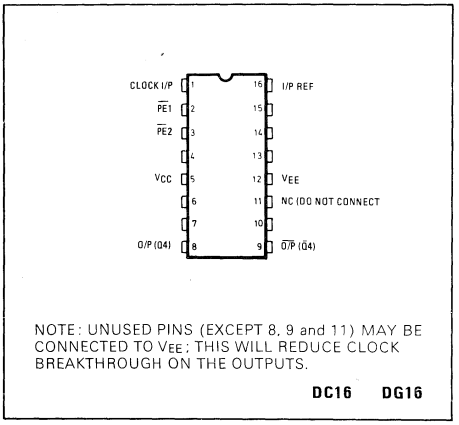
SP8748A, B & M
UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 8/9

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8748 series are UHF integrated circuits that can be logically programmed to divide by either 8 or 9 with input frequencies up to 300MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL III-compatible while the two complementary outputs are ECL-II compatible to reduce power consumption in the output stage. ECL III output compatability can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 8 when either $\overline{PE}$ input is in the high state and by 9 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

DC16 **DG16**

Fig. 1 Pin connections (top)

FEATURES

- Military and Industrial Variants
- 300 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Supply Voltage
  V_{CC} — V_{EE} 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

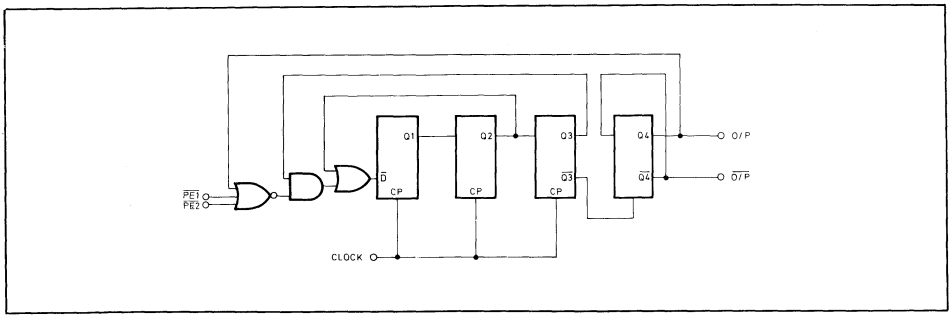


Fig. 2 Logic diagram (positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 'A' Variant −55°C to +125°C
'B' Variant 0°C to +70°C
'M' Variant −40°C to +85°C
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage evels					
V_{INH}	−1.10		−0.81	V	Tamb = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		K—	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3.
					I_{out} (external) = OmA
					(There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ±0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ±0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input voltage levels					
V_{INH}	−1.10		−1.10	V	T_{amb} = +25°C,
V_{INL}	−1.70		−1.50	V	see Note 4
Max. toggle frequency	300			MHz	
Min. frequency with sinewave clock input			10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz			20	V/μs	
Propagation delay (clock input to device output)		3		ns	
Set-up time		1.5		ns	See note 5
Release time		1.5		ns	See note 6

NOTES

4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷ 8 mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷9 mode is forced by that clock pulse (see Fig. 4).

Count Sequence			
Q_1	Q_2	Q_3	Q_4
L	H	H	H
L	L	H	H
H	L	L	L
H	H	L	L
L	H	H	L
L	L	H	L
L	L	L	H ← Extra state
H	L	L	H
H	H	L	H

Table 1 Count sequence

PE_1	PE_2	Div Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_3 or the H→L transition from $\overline{Q_3}$ is used to clock the stage controlling the ÷ 8/9. The loop delay is 8 clock periods minus the internal delays of the ÷ 8/9 circuit.

OPERATING NOTES

The SP8748 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

The ÷ 8/9 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7 gives the true output; the inverse can be obtained by interchanging the Q_3 and $\overline{Q_3}$ outputs.

The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 300MHz this would only leave about 16ns for the fully programmable counter to control the ÷ 8/9. The loop delay can be increased by extending the ÷ 8/9 function to, say, ÷ 16/17 or 32/33.

The SP8748 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase the noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

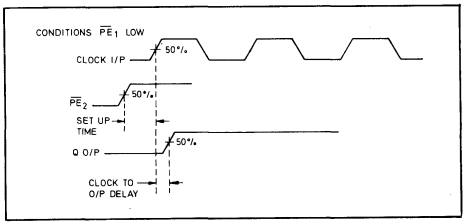


Fig. 3 Set-up timing diagram

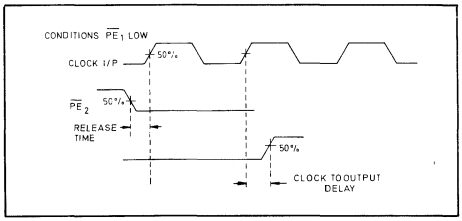


Fig. 4 Release timing diagram

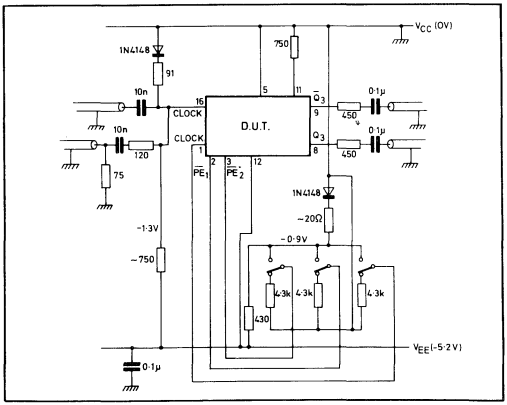


Fig. 5 Test circuit for dynamic measurements

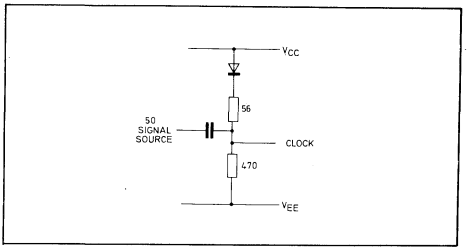


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source

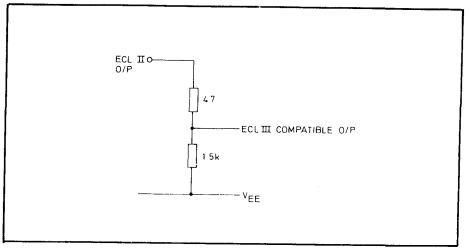


Fig. 8 ECL II to ECL III interface

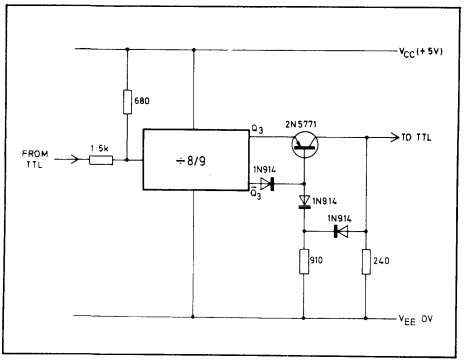


Fig. 7 TTL to ECL and ECL/TTL interfaces (SP874 devices and TTL operating from the same supply rails)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{in} (DC)	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	–55°C to +175°C

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP 8750 B,M 1.0 GHz
SP 8751 B,M 1.1 GHz
SP 8752 B 1.2 GHz

UHF ÷ 64 PRESCALERS

The SP8750 range of devices are ECL divide-by-sixtyfours which will operate at frequencies up to 1.2GHz.

The device has a typical power dissipation of 470mW at the nominal supply voltage of +6.8V.

FEATURES

- Input Ports for VHF and UHF
- Self-Biasing Clock Inputs
- Variable Input Hysteries Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input
- Push Pull TTL. O/P

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Band change input	+7.2 tc −0.5V or −10mA
Output current	+30 mA to −30 mA
Operating junction temperature	+150°C
Storage Temperature	−55°C to +150°C

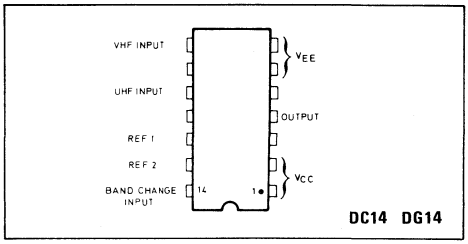


Fig. 1 Pin connections

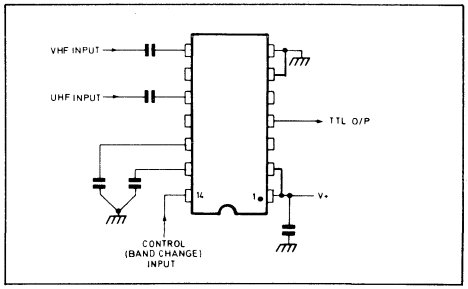


Fig. 2 Typical application

OPERATING NOTES

Two input ports are available on this device. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring on the other input at high frequencies. Both inputs are terminated by a nominal 400 and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1.2Hz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF1} - V_{REF2}$.

If the UHF input only is used and the device is required to operate with a sinewave input below 100 MHv, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The devices may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/μs.

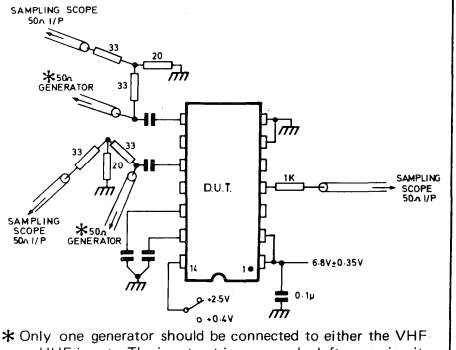
The divider is clocked on low to high transitions of either clock input.

ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90 mA max.
Temperature range: 'B' grade 0°C to +70°C, 'M' grade −40°C to +85°C
Clock inputs: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

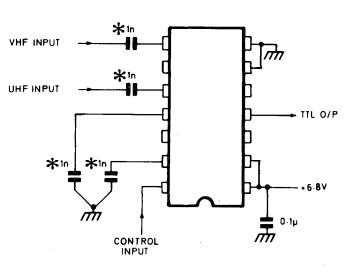
Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V
Clock input voltage: 400mV to 1.0Vp-p
T_{amb} = 0°C to +70°C ('B' grade), −40°C to +85°C ('M' grade)

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
UHF clock input						
Max. input frequency	SP8752	1.2			GHz	600mV p-p input
	SP8751	1.1			GHz	600mV p-p input
	SP8750	1.0			GHz	400mV p-p input
Min. input frequency	All			100	MHz	600mV p-p sinewave input
Min. slew rate for square wave input	All			200	v/μs	
VHF clock input						
Max. input frequency	All		1.0		GHz	
Min. input frequency			30	50	MHz	600mV p-p sinewave input
Band change input						
High level	All	2.5			V	
Low level				0.4	V	
Low level input current	All			0.8	mA	at 0.4V
Max. clamp current	All	−3			mA	at approx. −0.7V
Output						
High level	All	2.5	3.5	4.5	V	
Low level				0.4	V	5mA current sink
Supply current	All		68	90	mA	V_{CC} = 6.8V



* Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

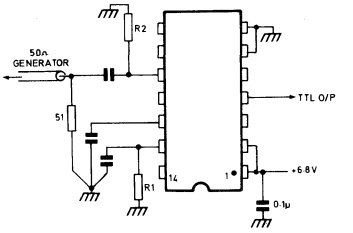
Fig. 3 AC test circuit



*Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

For single input operation leave pins 8 and 14 open circuit.

Fig. 4 Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.
For 50 mV hysteresis R1 = 36kΩ R2 = ∞
For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 Wideband operation

PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP8760 B & M
GENERAL PURPOSE SYNTHESISER CIRCUIT

The SP8760 is a multi-function device for use in phase-lock-loop systems. It contains a crystal oscillator maintaining circuit, followed by a divide-by-four stage; a digital phase/frequency comparator; and a two-modulus divider programmable to divide by 15 or 16.

It may be used with a prescaler to phase-lock single frequency transmitters or receivers in the HF, VHF or UHF bands.

The addition of an MOS/CMOS programmable plus fixed divider will generate a complete frequency synthesiser. The maximum frequency requirement of the control device is only 1 MHz, enabling complex functions to be performed using LSI technologies. With suitable prescalers, the controlled frequency source may extend into the IGHz region.

The SP8760 is available in two temperature grades: 0°C to +70°C ('B' grade) and −40°C to +85°C ('M' grade).

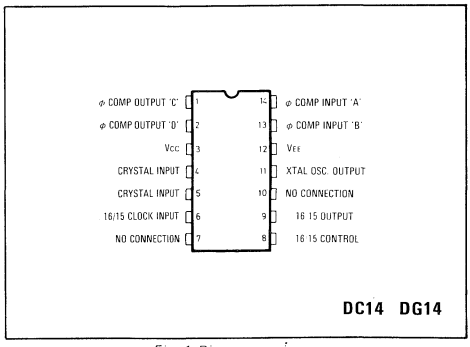


Fig. 1 Pin connections

FEATURES

- TTL/MOS Compatible Inputs and Outputs
- Low Power Consumption (<250mW Typ)
- Minimum External Components
- Voltage Pump Outputs on Phase/Frequency Comparator
- Zero Phase Difference Pulses <30nSec
- Crystal Oscillator Stability + 5 ppm at 4MHz, 0°C to + 70°C
- Crystal Oscillator Interfaces with SL680 for Very High Stability Applications

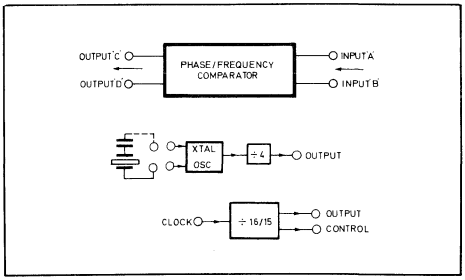


Fig. 2 SP8760 block diagram

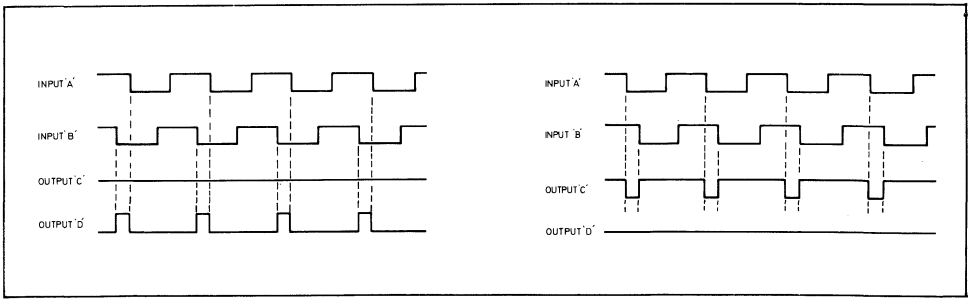


Fig. 3 Phase/frequency comparator waveforms

ELECTRICAL CHARACTERISTICS

Supply voltage 5V ± 0.5V
Supply current 45mA typ

Test conditions (unless otherwise stated):
V_{CC} = 4.5V to 5.5V
V_{EE} = 0V
T_{AMB} 0°C to +70°C ('B' grade)
−40°C to +85°C ('M' grade)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Power Supply Current		45	65	mA	
Crystal Osc. ÷4					
Crystal series capacitor		28		pF	•at 4MHz
Crystal series capacitor		20		pF	at 10 MHz
Temperature Stability			0.2	ppm/°C	at 4MHz, excluding crystal temperature coefficient.
Supply voltage stability		−1		ppm/V	at 4 MHz
External oscillator drive required		±1		mA	See Fig. 8.
Divide-by-four output, external current sink capability	5			mA	at 0.5V
Phase/Frequency Comparator					
Input current		250	350	uA	at Vin = 2.4V
Output 'C' current sink capability	6			mA	at 0.5V
Output 'D' current source capability	6				at (V_{CC} - 1.15V)
Zero phase pulse width			30	ns	
Input to Output delay		40		ns	
Divide by 16/15					
Control input current		250	350	µA	at Vin = 2.4V
Clock input current		−1.0	−1.6	mA	at Vin = 0.4V
Output external current sink capability	5			mA	at 0.5V
Maximum clock frequency	16	28		MHz	Divide by 16
	12	18		MHz	Divide by 15
Clock to output delay		35		ns	Output 1 - 0

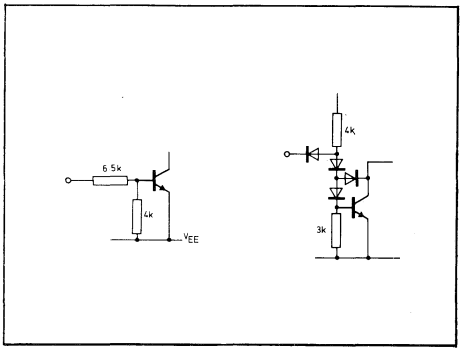


Fig. 4 Phase comp./divider control inputs

ABSOLUTE MAXIMUM RATINGS

Power supply V_{CC} − V_{EE} 0V to +10V
Output current 20mA
Operating junction temperature +150°C
Storage temperature −55°C to +150°C

OPERATING NOTES

The crystal oscillator is an emitter coupled circuit with an internal roll off capacitor to prevent oscillation at overtone frequencies. The crystal is connected in series with a capacitor between pins 4 and 5. It may be used with series resonant crystals at frequencies up to 10MHz. The stability of the crystal oscillator is better than ±5 p.p.m. at 4MHz over the temp range 0°C to 70°C (excluding the temperature coefficient of the crystal). If a higher stability is required the SL680 crystal oscillator maintaining circuit should be used. This may be interfaced to the SP8760 as shown in Fig. 8. The divide by four has a free collector output with an internal 2.5 KΩ resistor to Vcc.

The phase frequency comparator is an infinite pull-in range circuit which gives zero phase shift lock. The circuit triggers on the 1 - 0 edge of each input and gives an output which is proportional to the phase difference between the two edges (see Fig. 3). When the input 'A' edge precedes the input 'B' edge output 'C' will pulse to a low level while output 'D' will remain at a permanent low level. When the input 'B' edge precedes the input 'A' edge, output 'D' will pulse to a high level while output 'C' will remain at a permanent high level. The two outputs may be used to drive a charge pump and filler as shown in Figs. 5 and 6. The output of the filter may be used to drive directly the varactor line of a voltage controlled oscillator. For optimum 'noise' performance the output pulses from the phase detector must tend to zero when 'in lock'. The leakage on the filter output must therefore be kept to a minimum. If the varactor line draws a significant current it should be buffered using an emitter follower arrangement as shown in Fig. 7.

The phase/frequency comparator inputs are of the current source type as shown in Fig. 4. These may be driven by standard TTL or CMOS. Output 'C' is a free collector with an internal 10KΩ resistor to Vcc. Output 'D' is an emitter follower with an internal 10KΩ resistor to VEE.

The two-modulus prescaler may be controlled to divide by 16 or 15 using the control input. With the control input high the circuit will divide by 16. When a counter is used to control the two-modulus it should be clocked on the 1 - 0 edge of the 16/15 output. If the two-modulus is used only as a fixed divide-by-16 the control input - should be tied to Vcc. The prescaler clock input is a current sink input with a standard TTL fan in of one. It may be driven by standard or low power Schottky TTL. The control input is identical to the phase/frequency comparator inputs as shown in Fig. 4. The two modulus output is a free collector with an internal 1.5KΩ resistor to Vcc.

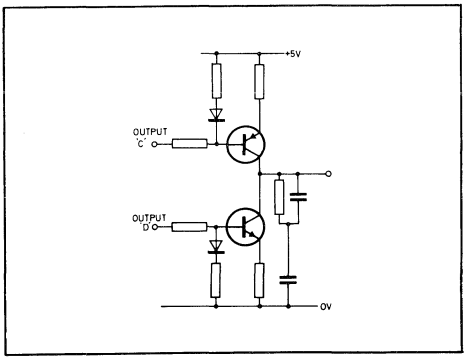


Fig. 5 Low voltage charge pump and filter
Divider clock input

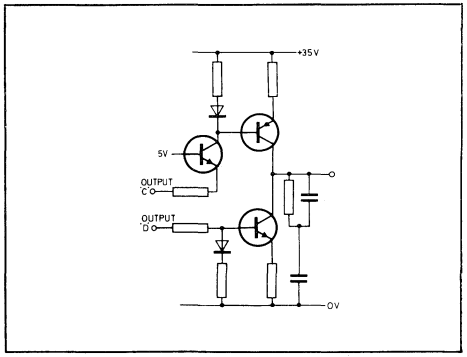


Fig. 6 High voltage charge pump and filter

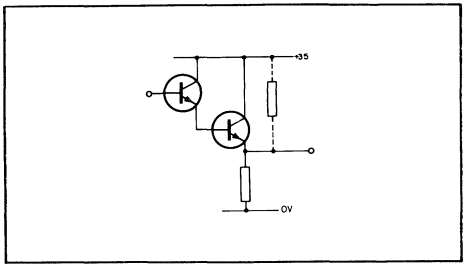


Fig. 7 Emitter follower buffer

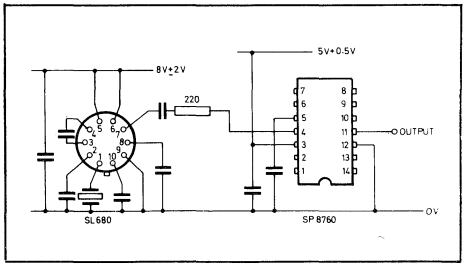


Fig. 8 SL680 to SP8760 interface

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8790 A, B & M
÷ EXTENDER FOR 2-MODULUS COUNTERS

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide-by-10 or 11 with the SP8790 becomes a divide-by-40 or 41, a divide by 5 or 6 becomes a divide by 20 or 21.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8790 into the region where CMOS or low power TTL can control the divider. The power-saving advantages are obvious.

The device interfaces easily to the SP8690 range of divide by 10 or 11s. The control inputs are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8790 is available in three temperature grades: 0°C to +70°C (SP8790B), −40°C to +85°C (SP8790-M) and −55°C to +125°C (SP8790A).

The SP8790 requires supplies of OV and +5V ±0.25V.

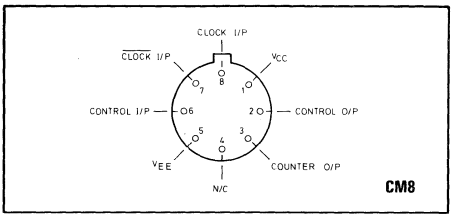


Fig. 1 Pin connections

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- I/P and O/P Interface Direct to CMOS/TTL

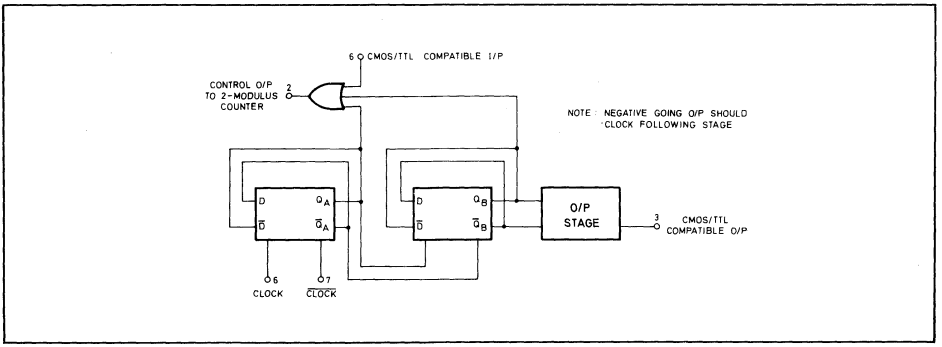


Fig. 2 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | VCC—VEE|	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating junction temperature	+150°C
Storage temp. range	−55°C to 150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: −55°C to +125°C (A grade)
−40°C to +85°C (M grade)
0°C to +70°C (B grade)
V_{CC} = −5V ± 5%
V_{EE} = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	See note 1			MHz	
Min toggle frequency with sine-wave input			20	MHz	See note 2
Min toggle frequency with square wave input	0			Hz	Slew rate 50V/µs
Clock to O/P delay (O/P − ve going)		14		ns	
Clock to O/P delay (O/P + ve going)		28		ns	
Control I/P to control O/P delay (O/P−ve going)		20		ns	10kΩ pulldown on control O/P (See note 5)
Clock I/P to control O/P delay (O/P+ve going)		10		ns	10kΩ pulldown on control O/P (See note 5)
Control I/P to control O/P delay (O/P−ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Control I/P to control O/P delay (O/P+ve going)		9		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P −ve going)		26		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P +ve going)		12		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P−ve going)		17		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P+ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Static					
Control I/P voltage level High state Low state	3.5 0		10 1.5	V V	See note 3
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (See note 4)					
Input impedance		1.6		kΩ	f_{in} = 0Hz
Input vias voltage ($\overline{CLOCK}$ and CLOCK)		2.4		V	Inputs open circuit
Power supply drain current		8.0	11	mA	

NOTES

1. The maximum frequency of operation is in excess of 60MHz when the SP8790 is used as a prescaler. The limitation on this maximum frequency is the saturating O/P stage. When the SP8790 is used as a controller its internal delays do not permit operation at frequencies in excess of 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-up resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695 with which the SP8790 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of the SP8640 series SP8745 and SP8746 with which the SP8790 can be used.

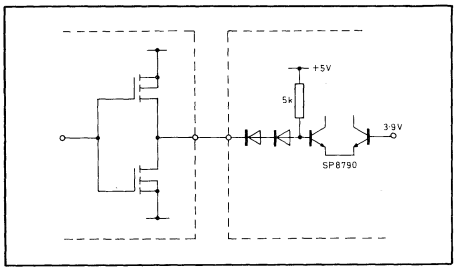


Fig. 3 CMOS and TTL compatible control input

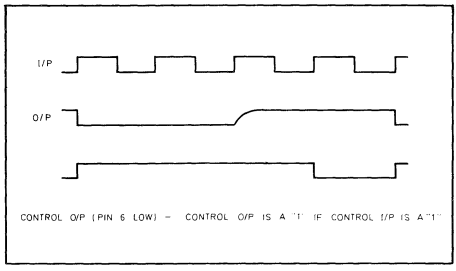


Fig. 4 SP8790 waveforms

OPERATING NOTES

The SP8790 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷40/41 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present. This may be prevented by using one of the arrangements shown in Fig. 6.

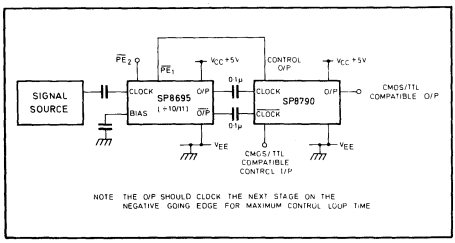


Fig. 5 SP8790 with SP8695 connected to give a ÷40/4

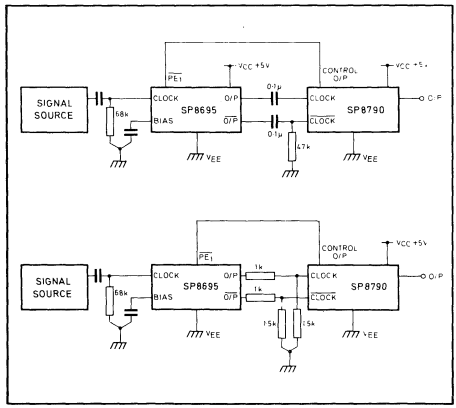


Fig. 6 Methods of preventing self-oscillation

TRUTH TABLE	
Control Input	**Div. Ratio With ÷10/11**
0	41
1	40

Max input frequency to combination=200MHz (min.).
Power consumption of combination=120mWtyp.
Time available to control the ÷40/41=(40 clock periods minus delays through the dividers) — 340ns (f_{in}=100MHz).

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8794 A,B & M
÷ 8 CONTROL CIRCUIT FOR 2 - MODULUS DIVIDERS

The SP8794 is a divide by eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide by 10 or 11 with the SP8794 becomes a divide by 80 or 81, a divide by 5 or 6 becomes a divide by 40 or 41.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8794 into the region where CMOS or low power TTL can control the divider.

The device interfaces easily to the SP8000 range of 2-modulus dividers. The control I/Ps are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8794 is available over three temperature ranges: 0°C to +70°C (SP8794B), −40°C to +85°C (SP8794M) and −55°C to +125°C (SP8794A).

The SP8794 requires supplies of 0V and +5V ± 0.25V

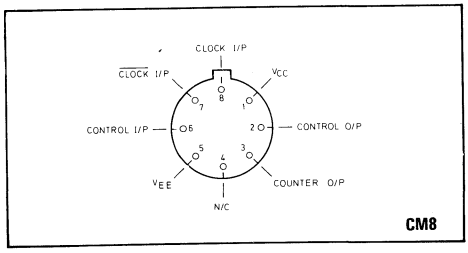


Fig. 1 Pin connections.

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- Direct I/P & O/P Interfacing to CMOS & TTL
- Operates with 500MHz ÷ 10/11

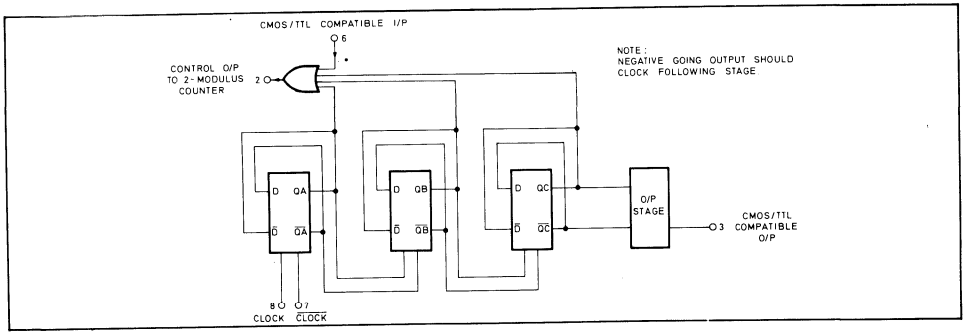


Fig. 2 Logic diagram.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating juntion temperature	+150°C
Storage temp. range	−55°C to 150°C

APPLICATION

- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C

V_{CC} = +5V ±5%

V_{EE} = 0V

Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	120			MHz	SP8794 as a prescaler (see note 1)
	40			MHz	SP8794 controlling a 2-modulus divider (see note 1)
Min. toggle frequency with sinewave input			20	MHz	See note 2
Min. toggle frequency with square wave input	0			Hz	Slew rate > 50V/μs
Clock to O/P delay (O/P −ve going)		18		ns	
Clock to O/P delay (O/P +ve going)		32		ns	
Control I/P to control O/P delay (O/P −ve going)		20		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P +ve going)		10		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P −ve going)		12		ns	4.3kΩ pulldown on O/P, see note 6
Control I/P to control O/P delay (O/P +ve going)		9		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P −ve going)		30		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P +ve going)		16		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P −ve going)		21		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P +ve going)		16		ns	4.3kΩ pulldown on O/P, see note 6
Static					
Control I/P voltage level					
High state	3.5		10	V	See note 3
Low state	0		1.5	V	
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (see note 4)			12	V	See note 4
Input impedance		1.6		kΩ	f_{in} = 0Hz
I/P bias voltage (CLOCK & $\overline{CLOCK}$)					
Power supply drain current					

NOTES

1. The maximum frequency of operation is in excess of 120MHz when the SP8794 is used as a prescaler. The limitation on its maximum operating frequency is the saturating output stage. When the SP8794 is used as a controller for a 2-modulus device its internal delays do not permit operation at frequencies above 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-out resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695, with which the SP8794 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of all the SP8640 series ÷ 10/11 devices, the SP8740 & SP8745 ÷ 5/6, the SP8741 & SP8746 ÷ 6/7 and the SP8743 ÷ 8/9, with which the SP8794 can be used.

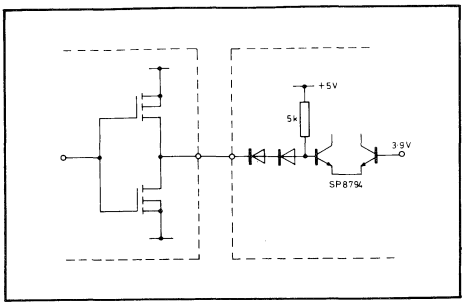


Fig. 3 CMOS and TTL compatible control I/P.

TRUTH TABLE	
Control I/P	**Div. Ratio with ÷ 10/11**
0	81
1	80

Max input frequency to combination = 200MHz (min.).
Power consumption of combination = 120mWtyp.
Time available to control the ÷ 80/81
= 80 clock periods minus delays through dividers
≅ 740ns (f_{in} = 100MHz)

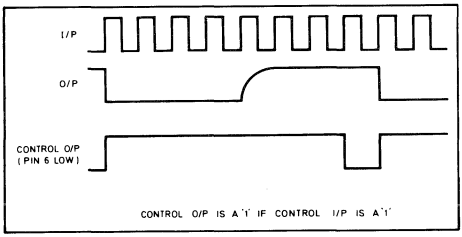


Fig. 4 SP8794 waveforms

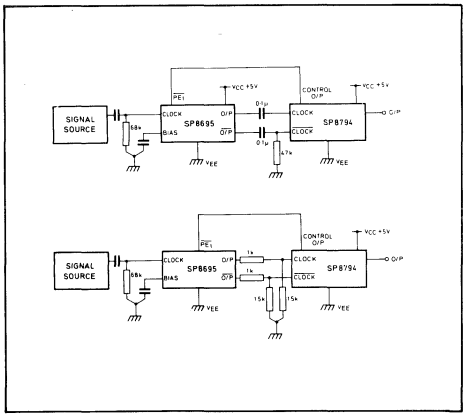


Fig. 6 Methods of preventing self-oscillation.

APPLICATION NOTES

The SP8794 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷ 80/81 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present, This may be prevented by using one of the arrangements shown in Fig. 6.

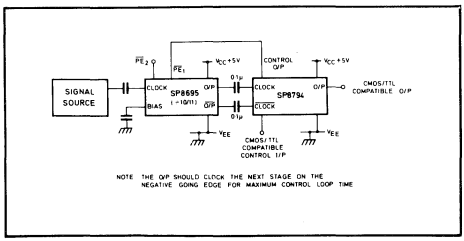


Fig. 5 SP8794 with SP8695 connected to give a low power ÷ 80/81

PLESSEY
SEMICONDUCTORS

SP1000/1200 SERIES
ECL II

The PECL II series of monolithic integrated logic circuits are a direct second source of the Motorola MECL II series. The family has been designed as a non-saturating form of logic so as to eliminate transistor storage time as a speed limiting characteristic and permit high speed operation.

PECL II circuits feature fast propagation delay times with commensurate rise and fall times, simultaneous complementary outputs, and excellent noise immunity as a result of near constant power supply drain.

FEATURES

- Propagation typically 4ns per logic decision.
- Excellent noise immunity characteristics
- Simultaneous OR/NOR outputs
- High fan-in and fan-out capabilities
- Internally temperature compensated

FUNCTIONS AND CHARACTERISTICS @ V_{CC} = 0V, V_{EE} = −5.2V, T_A = +25°C

Type		Function	DC output loading factor, each output	Propagation delay ns typ.	Total power dissipation mW typ.
0°C to +75°C	−55°C to +125°C				
SP1001	SP1201	Single 6 I/P gate, 3 OR O/P with pulldowns 3 NOR O/P with pulldowns	25	4.0	115
SP1004	SP1204	Dual 4-I/P gate, 2 OR with pulldowns 2 NOR with pulldowns			95
SP1007	SP1207	Triple 3-I/P gate, 3 NOR with pulldowns			110
SP1010	SP1210	Quad 2-I/P gate, 4 NOR with pulldowns		4.5	115
SP1013	SP1213	85 MHz a.c. coupled J-K flip-flop		6.0	125
SP1014	SP1214	Dual R-S flip-flop (+ve clock)			140
SP1015	SP1215	Dual R-S flip-flop (−ve clock)			
SP1016	SP1216	Dual R-S flip-flop (single rail, +ve clock)			
SP1020	SP1220	Quad line receiver		4.0	115
SP1023	SP1223	Dual 4-I/P OR/NOR clock driver		2.0	250
SP1026	SP1226	Dual 3-4I/P Transmission line and clock driver		2.0	140
SP1027	SP1227	120 MHz a.c. coupled J-K flip-flop		4.0	250
SP1030	SP1230	Quad exclusive OR gate		5.0	130
SP1031	SP1231	Quad exclusive NOR gate		5.0	130
SP1032*	SP1232*	100 MHz a.c. coupled Dual J-K flip-flop		4.5	180
SP1033	SP1233	Dual R-S flip-flop (single rail, −ve clock)		6.0	140
SP1034	SP1234	Type D flip-flop		4.0	185
SP1035	SP1235	Triple line receiver		5.0	140
SP1039*	SP1239*	Quad level translator (PECL to saturated logic)	7 (DTL)	12	200
SP1048	SP1248	Quad 2-I/P NAND gate	25	5.0	130

* In 16– lead D.I.L. All other types are in 14– lead D.I.L.

GENERAL PARAMETERS

Common Characteristics

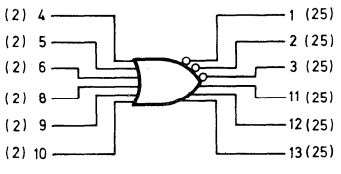
Characteristic	SP1200						SP1000					
	–55°		+25°C		+125°C		0°C		+25°C		+75°C	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Input current I_{in}				100μA						100μA		
Input leakage I_R				0.2μA		1μA				0.2μA		1μA
Output voltage[2]												
Logic '1' (V_{OH})	–0.990	–0.825	–0.85	–0.70	–0.70	–0.53	–0.895	–0.74	–0.85	–0.70	–0.775	–0.615
Logic '0' (V_{OL})	–1.89	–1.58	–1.8	–1.5	–1.72	–1.38	–1.83	–1.525	–1.8	–1.5	–1.76	–1.435

NOTES
1. The above characteristics apply unless otherwise stated under individual product information.
2. Outputs without pulldown resistors are tested with 1.5kΩ resistor to V_{ee} and V_{OH} limits apply from no load (0 mA) to full load (–2.5 mA).
3. General parameters only apply to basic gates and flip-flops.

Test Conditions

Test Temp. °C	Test Voltage/Current Values						
	V_{IL} (V)		V_{IH} (V)		V_{IH} (max.) (V)	Vee (V)	I_L (m.Ad.c.)
	Min.	Max.	Min.	Max.			
–55	–5.2 to –1.405		–1.165 to –0.825		–	–5.2	–2.5
+25	to –1.325		–1.025 to –0.700		–0.700		
+125	to –1.205		–0.875 to –0.530		–		
0	to –1.350		–1.070 to –0.740		–		
+25	to –1.325		–1.025 to –0.700		–0.700		
+75	to –1.260		–0.950 to –0.615		–		

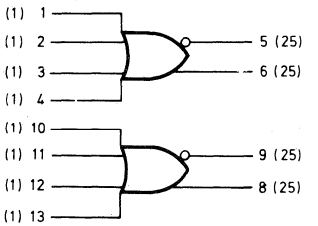
SP1001/SP1201
6-INPUT GATE



$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$
$11 = 4 + 5 + 6 + 8 + 9 + 10$

t_{pd} = 4.0 ns
P_D = 115 mW

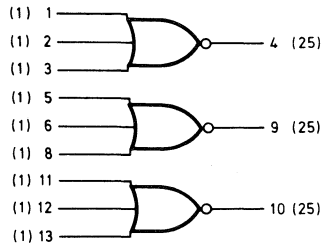
SP1004/SP1204
DUAL 4-INPUT GATE



$5 = \overline{1 + 2 + 3 + 4}$
$6 = 1 + 2 + 3 + 4$

t_{pd} = 4.0ns
P_D = 95mW

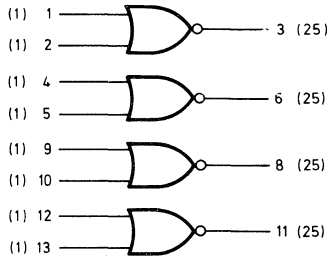
SP1007/SP1207
TRIPLE 3-INPUT GATE



$4 = \overline{1 + 2 + 3}$

t_{pd} = 4.0 ns
P_D = 110 mW

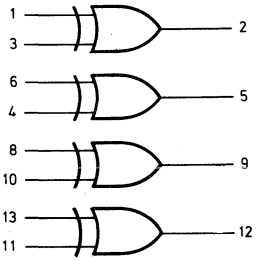
SP1010/SP1210
QUAD 2-INPUT NOR GATE



$3 = \overline{1 + 2}$

t_{pd} = 4.5ns
P_D = 115mW

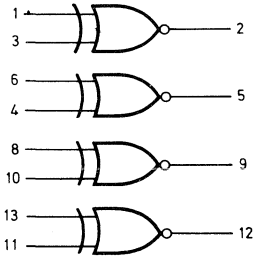
SP1030/SP1230
QUAD EXCLUSIVE OR GATE



$2 = 1 \bullet \overline{3} + \overline{1} \bullet 3$

DC Input Loading Factor:
Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
t_{pd} = 5.0 ns typ
Power Dissipation = 130 mW typ

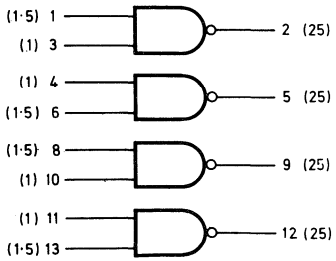
SP1031/SP1231
QUAD EXCLUSIVE NOR GATE



$2 = 1 \bullet 3 + \overline{1} \bullet \overline{3}$

DC Input Loading Factor:
Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
Power Dissipation = 130 mW typ
t_{pd} = 5.0 ns typical

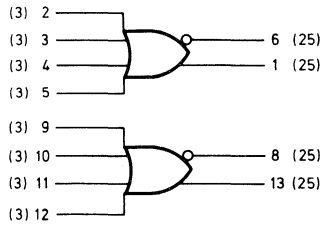
SP1048/SP1248
QUAD 2-INPUT NAND GATE



$2 = \overline{1 \bullet 3}$

t_{pd} = 5.0 ns
P_D = 130 mW

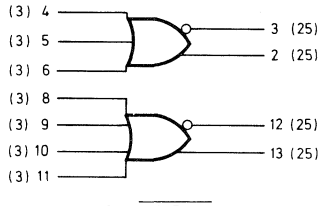
SP1023/SP1223
DUAL 4-INPUT CLOCK DRIVER



$6 = \overline{2 + 3 + 4 + 5}$
$1 = 2 + 3 + 4 + 5$

t_{pd} = 2.0 ns
P_D = 250 mW
N.M. = 150 mV

SP1026/SP1226
DUAL 3-4-INPUT TRANSMISSION LINE AND CLOCK DRIVER

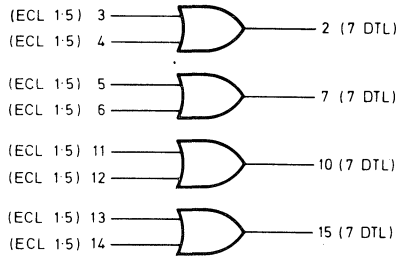


$3 = \overline{4 + 5 + 6}$

$2 = 4 + 5 + 6$

t_{pd} = 2.0 ns
P_D = 140 mW
N.M. = 150 mV

SP1039/SP1239
QUAD LEVEL TRANSLATOR

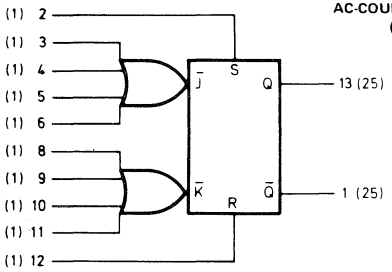


$2 = 3 + 4$

t_{pd} = 12 ns
P_D = 200 mW

Power supply connections:
Pin 1 = +5.0V
Pin 8 = −5.2V
Pin 16 = 0V

SP1013/SP1213
AC-COUPLED J–K FLIP/FLOP (85 MHz TYP.)



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels whereas the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to logic '1' only while $\overline{C}_D$ is in the logic '1' state. ($\overline{C}_D$ maximum '1' level = V_{CC} −0.6V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

t_{pd} = 6.0 ns
P_D = 125 mW

CLOCKED J–K OPERATION

$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^{n+1}
ø	ø	⎍	Q^n
0	0	⎍	$\overline{Q}^n$
0	1	⎍	1
1	0	⎍	0
1	1	⎍	Q^n

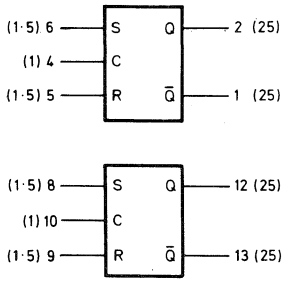
ø = Don't care

R–S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	ND

ND = Not defined

SP1014/SP1214
DUAL CLOCKED R–S FLIP/FLOP (POSITIVE CLOCK)



SP1015/SP1215
DUAL CLOCKED R–S FLIP/FLOP (NEGATIVE CLOCK)

SP1014/1214

C	R	S	Q^{n+1}
1	0	0	Q^n
1	0	1	1
1	1	0	0
1	1	1	ND
0	ø	ø	Q^n

ø = Don't care

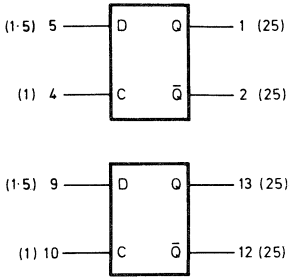
SP1015/1215

C	R	S	Q^{n+1}
0	0	0	Q^n
0	0	1	1
0	1	0	0
0	1	1	ND
1	ø	ø	Q^n

ND = Not defined

t_{pd} = 6.0 ns
P_D = 140 mW

SP1016/SP1216
DUAL CLOCKED, SINGLE RAIL
R–S FLIP/FLOP
(NEGATIVE CLOCK)



t_{pd} = 6.0 ns
P_D = 140 mW

SP1033/SP1233
DUAL CLOCKED, SINGLE RAIL
R–S FLIP/FLOP
(POSITIVE CLOCK)

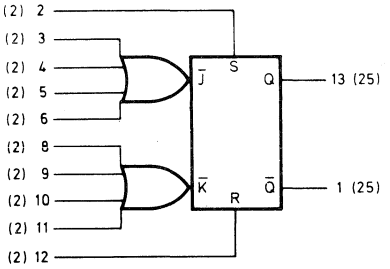
SP1016/1216

C	D	Q^{n+1}
0	0	Q^n
0	1	Q^n
1	0	0
1	1	1

SP1033/1233

C	D	Q^{n+1}
1	0	Q^n
1	1	Q^n
0	0	0
0	1	1

SP1027/SP1227
AC-COUPLED J–K FLIP/FLOP
(127 MHz TYP.)



CLOCKED J–K OPERATION

$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^{n+1}
ø	ø	⎍	Q^n
0	0	⎍	$\bar{Q}^n$
0	1	⎍	1
1	0	⎍	0
1	1	⎍	Q^n

ø = Don't care

R–S OPERATION

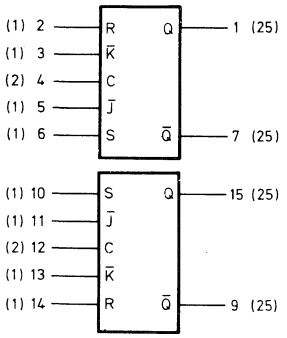
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	ND

ND = Not defined

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels whereas the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to logic '1' only while $\bar{C}_D$ is in the logic "1" state. ($\bar{C}_D$ maximum '1' level = V_{CC} –0.6V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

t_{pd} = 4.0 ns
P_D = 250 mW

SP1032/SP1232
100MHz, AC-COUPLED
DUAL J–K FLIP/FLOP



CLOCKED $\overline{J}$–$\overline{K}$ TRUTH TABLE

$\overline{J}$	$\overline{K}$	Clock	Q^n
*	*	4 & 12	1 & 15
Δ	Δ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

* Any $\overline{J}$ or $\overline{K}$ input
All other $\overline{J}$ – $\overline{K}$ inputs and the R–S inputs are at a 'O' Level
Δ = Either logic level will result in the desired output.

$\overline{J}_D$ – $\overline{K}_D$ TRUTH TABLE

Pin No.

$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
*	*	1 & 15
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q}^n$

All Clock/R–S inputs are at a 'O' Level.

R–S TRUTH TABLE

Pin No.

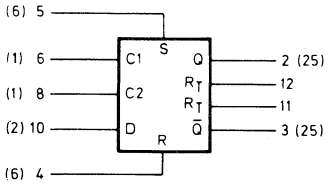
R	S	Q^{n+1}
2 & 14	6 & 10	1 & 15
0	0	Q^n
0	1	1
1	0	0
1	1	ND

All $\overline{J}$–$\overline{K}$ inputs and Clock inputs are static
ND = Output state not defined

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the clock input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logic '1' only while the clock input is in a logic '1' state (Clock maximum '1' level = V_{CC} –0.7V).

$t_{pd} \simeq 4.5$ns
$P_D = 180$mW
NM = 150mV

SP1034/SP1234
TYPE D FLIP/FLOP



P_D = 185 mW using external 600Ω pulldown resistors
= 240 mW using internal pulldown resistors.

R–S TRUTH TABLE

Pin No.

R	S	Q^{n+1}	$\overline{Q}^{n+1}$
4	5	2	3
0	0	Q^n	$\overline{Q}^n$
0	1	1	0
1	0	0	1
1	1	ND	ND

ND = Not defined

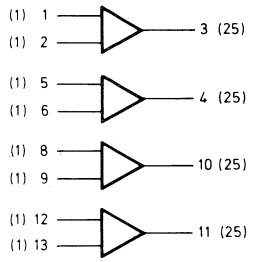
CLOCKED TRUTH TABLE

Pin No.

D	C	Q^{n+1}	$\overline{Q}^{n+1}$
10	6 or 8	2	3
0	0	Q^n	$\overline{Q}^n$
1	0	Q^n	$\overline{Q}^n$
0	1*	0	1
1	1*	1	0

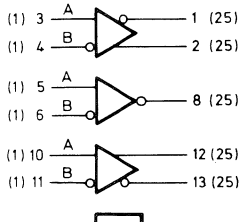
* A '1' or clock input is defined for this flip-flop as a change in level from low to high.

SP1020/SP1220
QUAD LINE RECEIVER



t_{pd} = 4.0 ns
P_D = 115 mW

SP1035/SP1235
TRIPLE LINE RECEIVER



t_{pd} = 5.0 ns
P_D = 140 mW

TRUTH TABLE

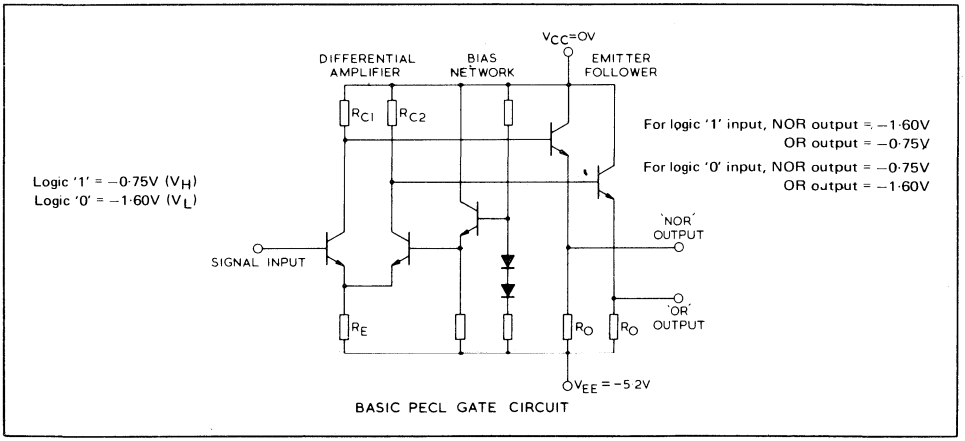
INPUTS		OUTPUTS	
A	B	OR	NOR
1	V_{BB}	1	0
0	V_{BB}	0	1
V_{BB}	1	0	1
V_{BB}	0	1	0

LOGIC DIAGRAMS

The logic diagrams describe the circuits of the PECL II series and permit quick selection of those circuits required to implement a particular logic system. The Logic equations and truth tables shown with the logic diagrams, together with typical propagation delay times (t_{pd}) and typical power dissipation per package given in the characteristics table demonstrate series compatibility.

Package pin numbers are identified by numbers directly adjacent to the device terminals, whereas the numbers in parentheses indicate d.c. loading factors at each terminal. PECL II circuits contain internal bias networks, ensuring that the transition point is always in the centre of the transfer characteristic curves over the temperature range.

V_{CC} = pin 14 and V_{EE} = pin 7 for all devices (14-lead D.I.L.) except SP1032/1232, and SP1039/1239 where V_{CC} = pin 16 and V_{EE} = pin 8 (16-lead D.I.L.)



BASIC PECL GATE CIRCUIT

CIRCUIT DESCRIPTION

The PECL II line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical PECL II circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

As shown in the schematic diagram above, it is recommended that −5.2V be applied at V_{EE} with V_{CC} = Gnd.

SYSTEM LOGIC SPECIFICATIONS

The nominal output logic swing of 0.85 V then varies from a low state of V_L = −1.60 V to a high state of V_H = −0.75 V with respect to ground.

If Positive logic is used when reference is made to logical zeros or ones then

'0' = −1.60 V
'1' = −0.75 V typical

Dynamic logic refers to a change of logic states. Dynamic '0' is a negative going voltage excursion and a dynamic '1' is a positive going voltage excursion.

CIRCUIT OPERATION

An internal bias of −1.175 V is applied to the 'bias input' of the differential amplifier and the logic signals are applied to the 'signal input'. If a logical '0' is applied, the current through R_E is supplied by the internally biased transistor. A drop of 0.85 V occurs across R_{C2}. The OR output then is −1.60 V, or one V_{BE} drop below 0.85 V. Since no current flows in the 'signal input' transistor, the NOR output is a V_{BE} drop below ground, or −0.75 V. When a logical '1' level is applied to the 'signal input' the current through R_{C2} is switched to the 'signal input' transistor and a drop of 0.85 V occurs across R_{C1}. The OR output then goes to −0.75 V and the NOR output goes to −1.60 V.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from an internal regulated, temperature compensated bias network. The temperature characteristics of the bias network compensate for any variations in circuit operating point over the temperature range or supply voltage changes, and ensure that the threshold point is always in the centre of the transfer characteristic curves.

ABSOLUTE MAXIMUM RATINGS

Ratings above which device life may be impaired

Power supply voltage (V_{CC} = 0)	(V_{ee})	−10V d.c.
Input voltage (V_{CC} = 0)	(V_{in})	0 to V_{ee}
Output source current	(I_O)	20mA d.c.
Storage temperature range	($T_{stg.}$)	−65°C to +175°C

Recommended Maximum ratings above which performance may be degraded

Operating temperature range	
SP1000	0°C to +75°C
SP1200	−55°C to +125°C
A.C. fanout* (gates and flip-flops)	15

Minimum d.c. fanout is guaranteed at 25; an a.c. fanout of 15 is recommended for high-speed operation.

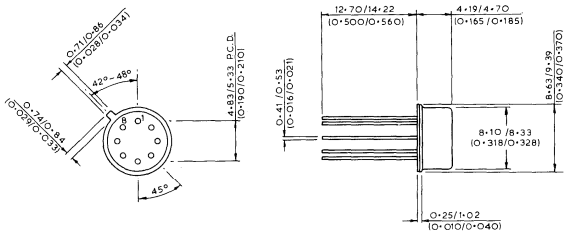
packages

package outlines

Dimensioned outline diagrams of the packages currently available for standard products are given on this and the following pages. Whilst every effort is made to ensure that the packages offered conform to these diagrams, certain changes may occur from time to time dependent on the supplies of piece parts. However, Plessey Semiconductors will attempt to ensure that such changes, should they occur, shall be minimal.

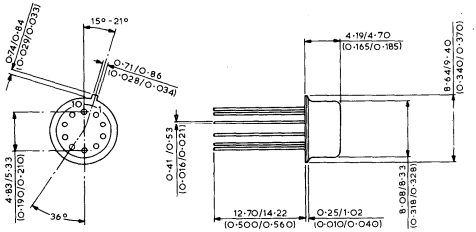
The code used to identify package outlines is that shown on the appropriate datasheet and on the following diagrams. The Pro-Electron code (see Ordering Information) is used – with the addition of numerals indicating the number of leads.

Note: Dimensions are shown thus: mm (inches)



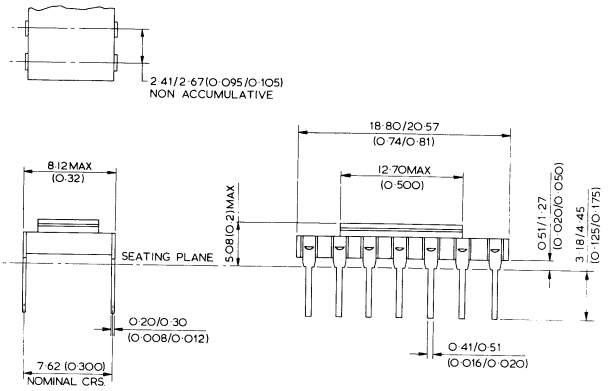
8 LEAD TO–5

CM8



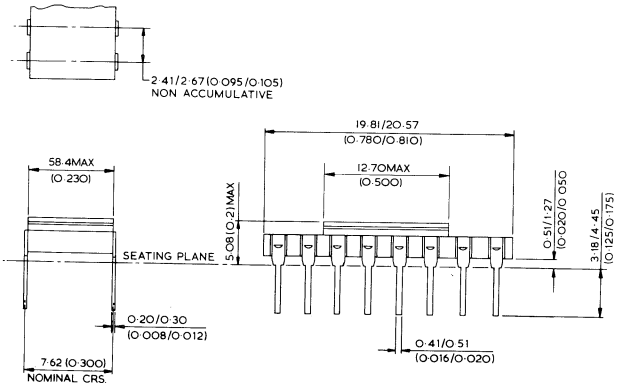
10 LEAD TO–5

CM10



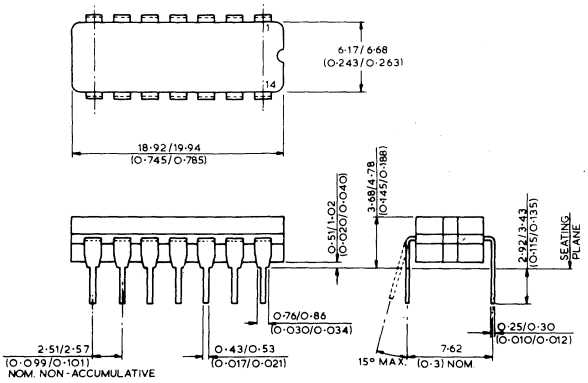
14 LEAD DILMON

DC14



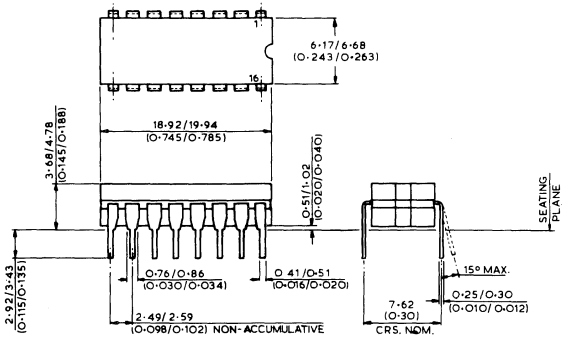
16 LEAD DILMON

DC16



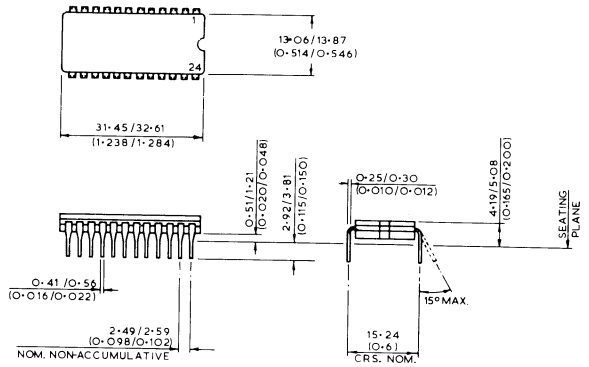
14 LEAD CERAMIC DIL

DG14



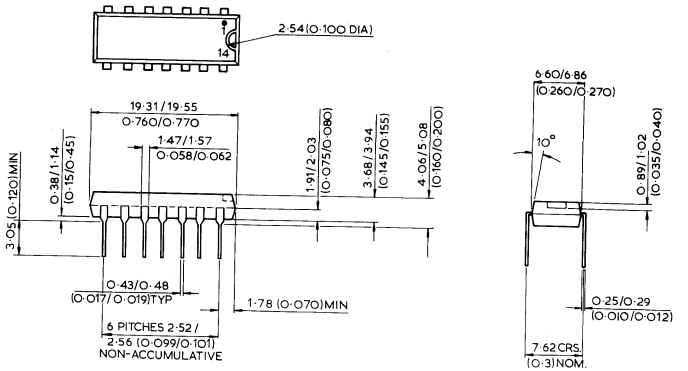
16 LEAD CERAMIC DIL

DG16



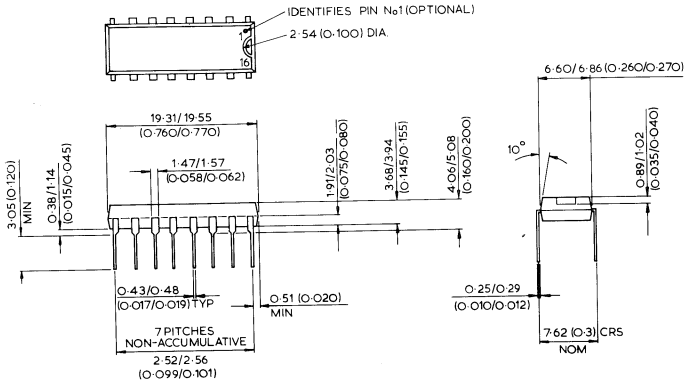
24 LEAD CERAMIC DIL

DG24



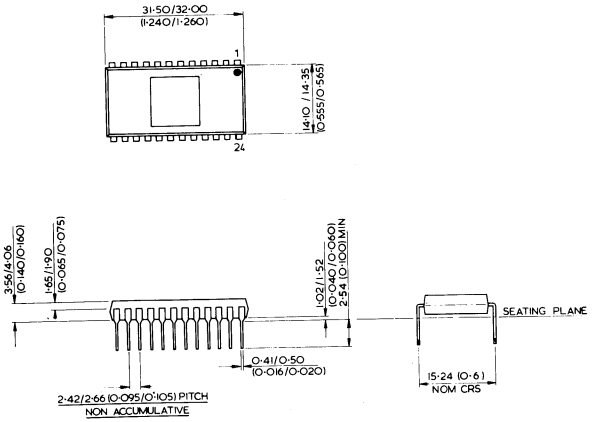
14 LEAD PLASTIC DIL

DP14



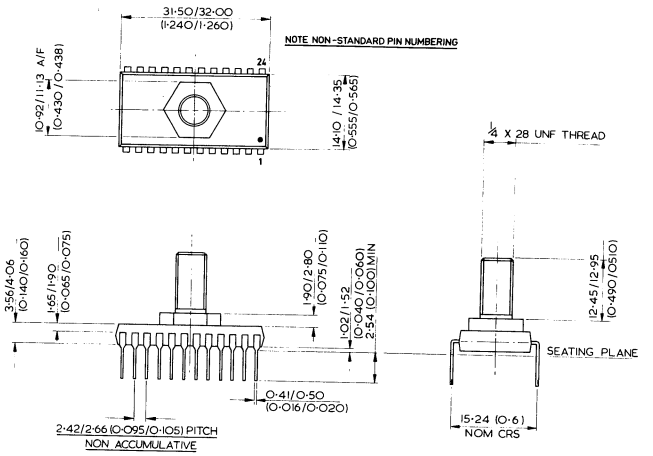
16 LEAD PLASTIC DIL

DP16



24 LEAD PLASTIC DIL

DP24



24 LEAD PLASTIC DIL WITH HEAT SINK STUD

DP24

ordering information

ordering information

U.K. ORDERS

Orders for quantities up to 99 received by Plessey Semiconductors at Swindon will be referred automatically to our U.K. distributors; quantities of 1000 and over must be ordered from Plessey Semiconductors direct, at the following address:

Plessey Semiconductors
Cheney Manor
Swindon
Wilts. SN2 2QW
Tel: (0793) 36251
Telex: 449637

OVERSEAS ORDERS

Products contained in this Databook can be ordered from your listed Plessey Office. Agent or Distributor.

PLESSEY SEMICONDUCTORS IC TYPE NUMBERING

Plessey Semiconductors integrated circuits are allocated type numbers which must be used when ordering. The Pro-Electron code is used to identify package outlines.

CM – Multilead TO-5
DC – Dilmon
DG – Ceramic Dual In-Line
DP – Plastic Dual In-Line
EP – Power Stud

This package code is for reference purposes only and need only be used when ordering where a device is offered in more than one package style. The package code does not appear on the device itself.

Plessey Semiconductors world-wide

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FRANCE Plessey France S.A., 16/20 Rue Petrarque, 75016 Paris. Tel: 727 43 49 Tx: 62789

ITALY Plessey S.p.A., Corso Sempione 73, 20149 Milan. Tel: 349 1741 Tx: 37347

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